Lattice ECC for NAND Flash Memory

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ECC for NAND Flash Memory

- The challenges facing ECC for NAND are well understood
- As information density increases (e.g. sub 20-nm process), cells become less reliable and stronger ECC is needed to achieve performance
- We believe it is necessary to design ECC specifically to suit NAND flash memory rather than lifting directly from other storage tech. (e.g. HDD)
- Here we present a new ECC architecture based on a lattice structure that is optimized for NAND flash memory

Lattice ECC – Technical Spec.

ECC Type:	BCH	LDPC	LATTICE
Decoder Type	Hard	Soft	Hard or Soft
RAW BER[1]	$3x10^{-3}$	?	$2x10^{-2}$
uPER Eval.	Easy	Hard	Easy
Complexity[2]	O(N log(N))	O(N)	O(N)
Error Floor	No	Yes	*Hard Mode:* No *Soft Mode:* lower than LDPC

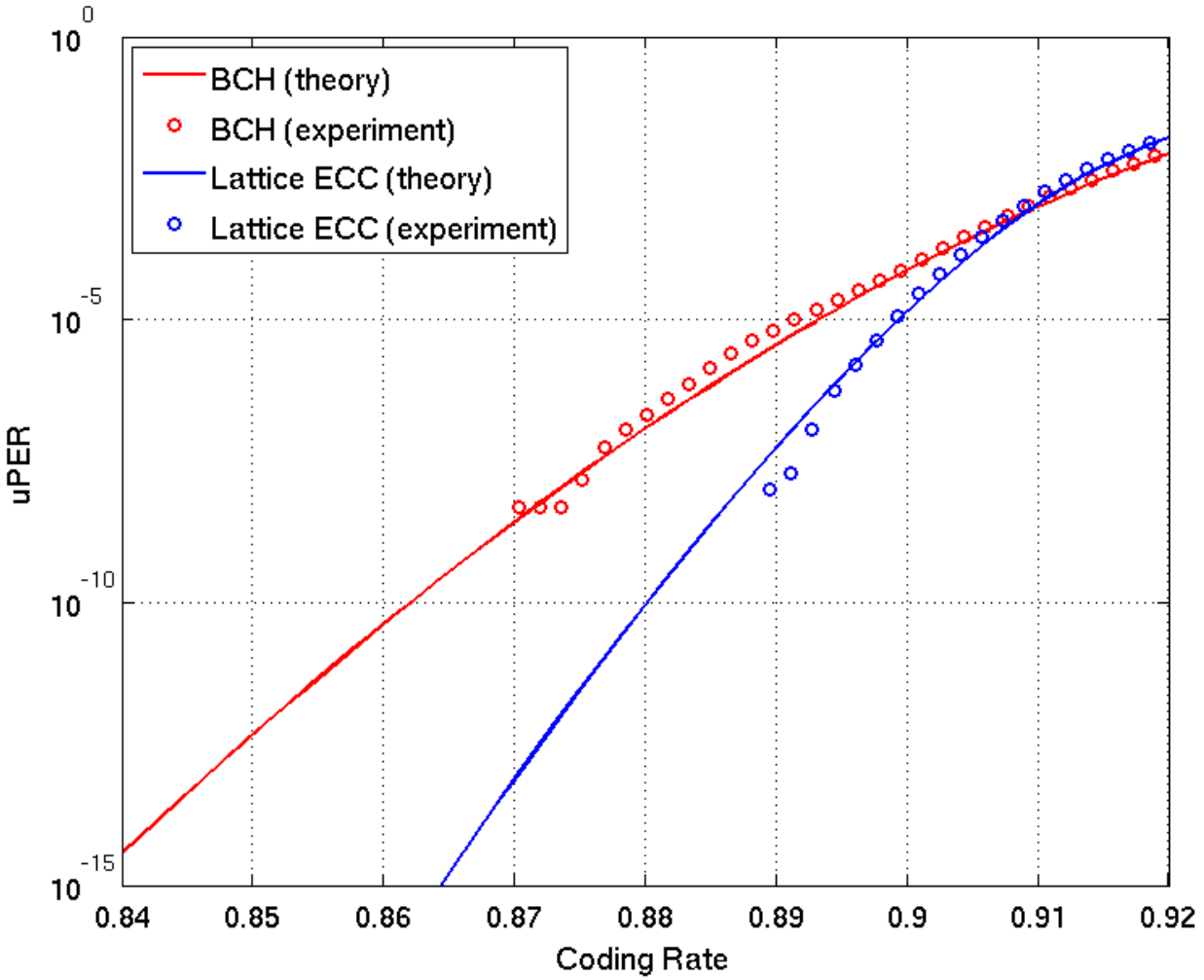
[1] - RAW BER required to achieve operational PER=10^{-15} over Gaussian MLC channel with overall coding rate=0.85

[2] – Complexity in terms of code block length (there are of course other considerations for implementation e.g. number of BP iterations)

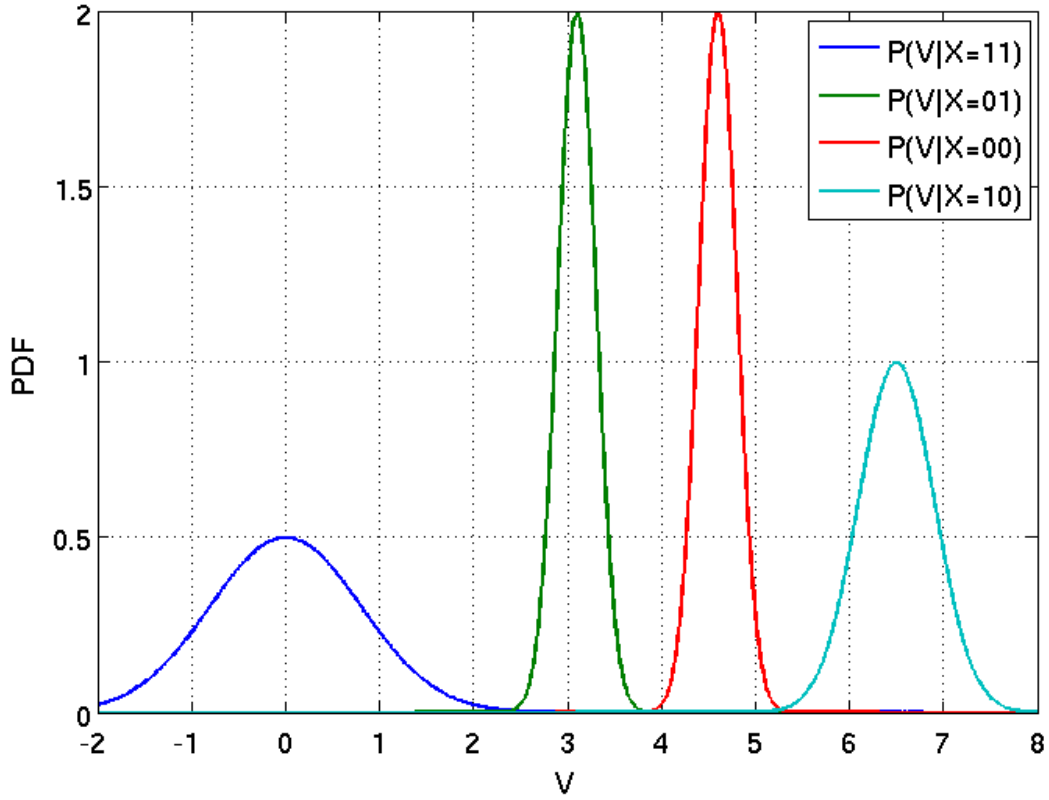
uPER Evaluation

- MLC 25nm NAND
- 6000 random program/erase cycles (applied according to JEDEC standard)
- 10 years data retention time
- Close to 1 billion pages captured using SigNas II software + FPGA

Experiment matches theory closely down to very low uPER!



Gaussian MLC Channel



- X – programmed state
- Cell Voltage Levels
  - $V|X=11 \sim N(\mu_{11}, s_{11})$
  - $V|X=01 \sim N(\mu_{01}, s_{01})$
  - $V|X=00 \sim N(\mu_{00}, s_{00})$
  - $V|X=10 \sim N(\mu_{10}, s_{10})$

Repeated applications of NAND RR feature can produce soft-outputs that approach LLRs given by this model (or similar)

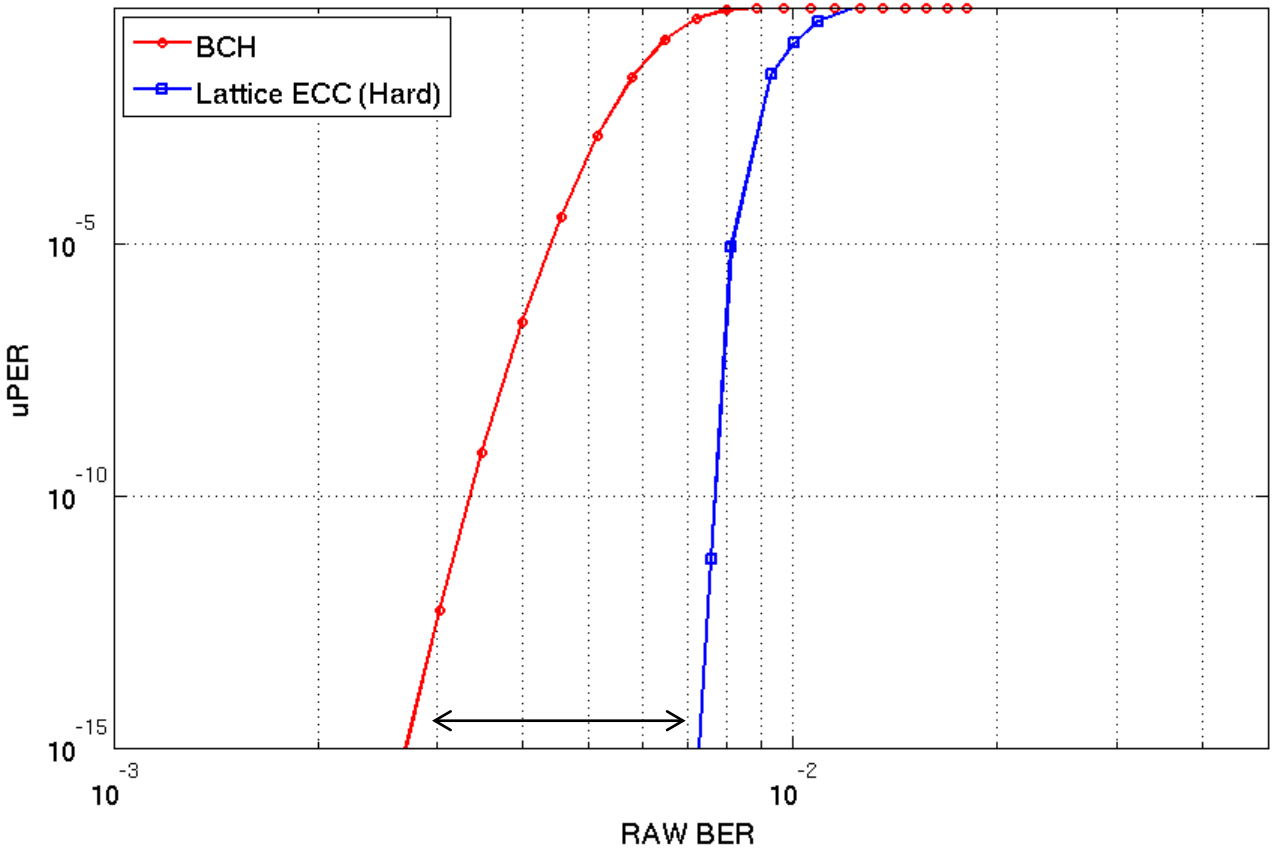
$$LLR_U = log\left(\frac{0.5\Pr(V|X=10) + 0.5\Pr(V|X=11)}{0.5\Pr(V|X=00) + 0.5\Pr(V|X=01)}\right)$$

$$LLR_L = log\left(\frac{0.5\Pr(V|X=01) + 0.5\Pr(V|X=11)}{0.5\Pr(V|X=00) + 0.5\Pr(V|X=10)}\right)$$

Demonstration – Hard Mode

- Code block length N=8192
- All schemes have coding rate R=0.847
- BCH is t=97 bit correctable

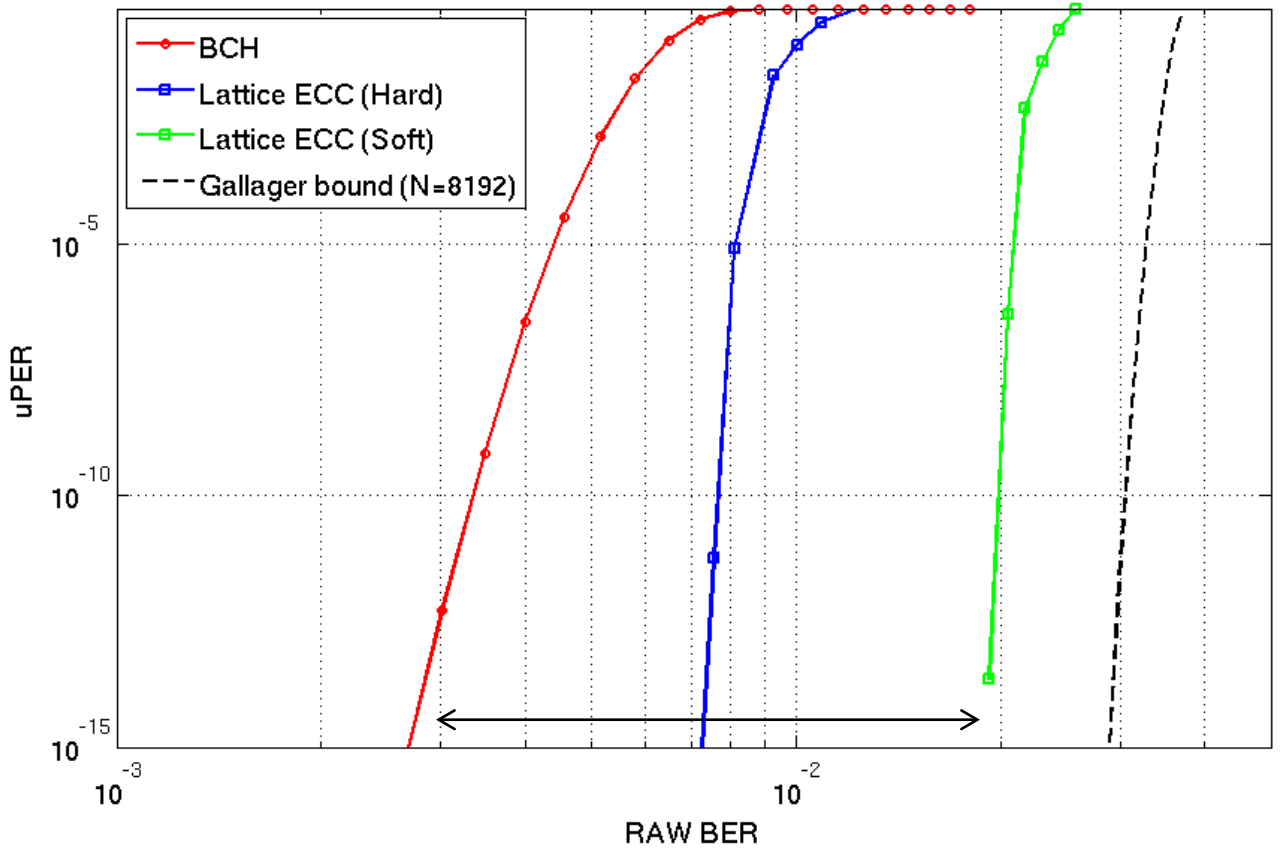
Lattice ECC (hard mode) can achieve uPER=10^{-15} with around **2x increase** in RAW BER compared with BCH



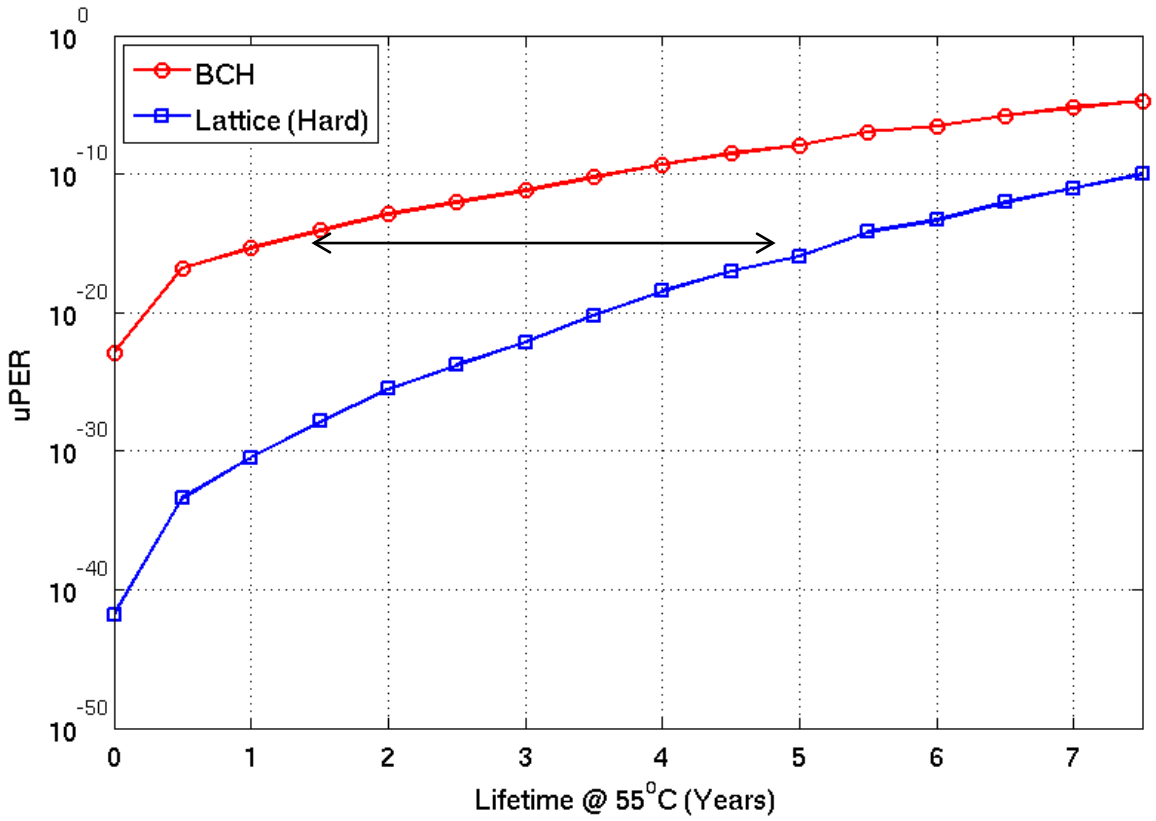
Demonstration – Soft Mode

- Code block length N=8192
- All schemes have coding rate R=0.847
- BCH is t=97 bit correctable

Lattice ECC (soft mode) can achieve uPER=10^{-15} with around **7x increase** in RAW BER compared with BCH



Demonstration – Lifetime Gain



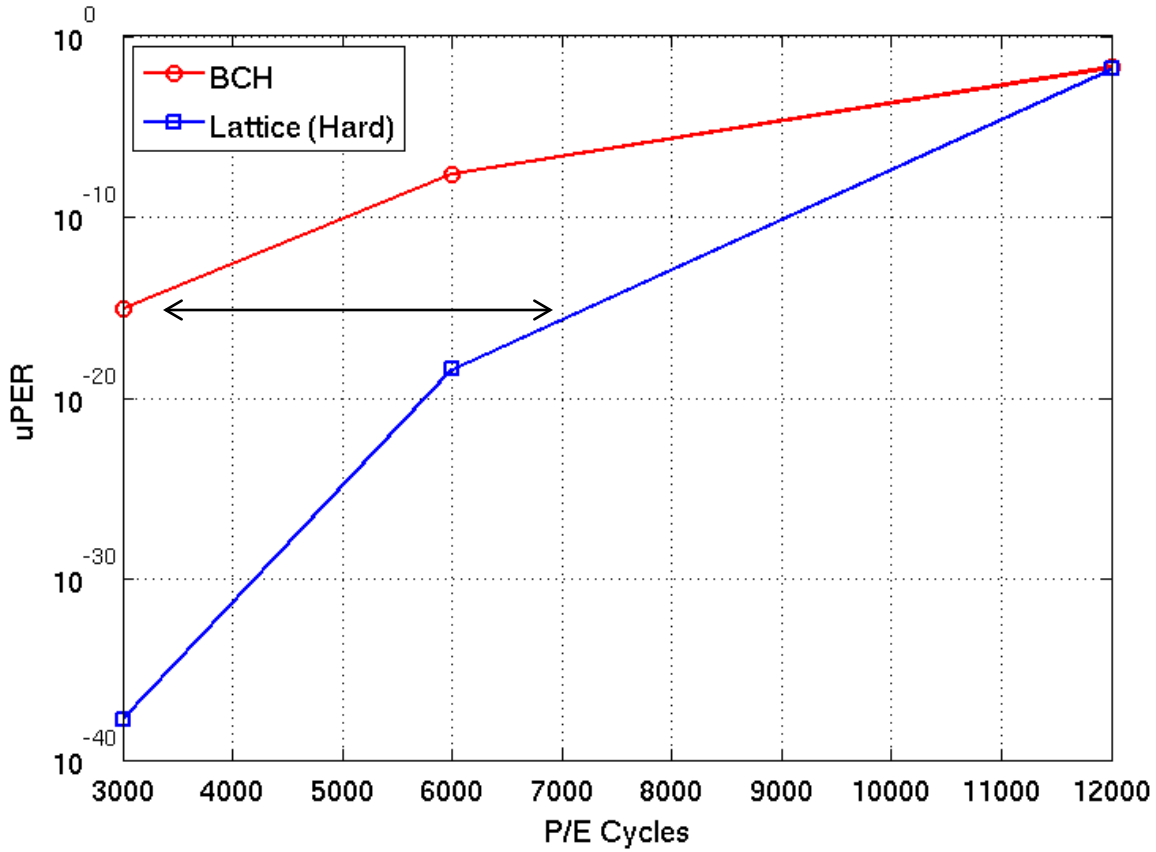
- MLC 25nm NAND
- 3000 random program/erase cycles
- Baked at 145°C at uniform intervals
- Arrhenius law (E_A=1.1eV) is used to calculate equivalent time at 55°C
- Code block length N=8192+224(ecc)
- Both schemes have coding rate R=0.97

Lattice ECC lasts **for 5x as long** before uPER crosses 10^{-15} threshold

Demonstration – PE Cycle Gain

- MLC 25nm NAND
- Bake equivalent to 1.1 years at 55°C
- Code block length N=8192+238(ecc)
- Both schemes have coding rate R=0.97

Lattice ECC can withstand **2x as many** PE cycles before uPER crosses 10^{-15} threshold



Conclusions

- A new ECC architecture based on *lattice structure* optimized for NAND flash memory
- Decoder has both algebraic structure and probabilistic elements
- No significant increase in complexity or R/W throughput
- Simple method for evaluating operational uPER
- Hard Mode:
  - 2x gain in RAW BER
  - 2x as many P/E cycles
  - 5x improvement in lifetime
- Soft Mode:
  - 7x gain in RAW BER
- *Technical details of algorithm will be revealed once patent process is completed (or under NDA)*