Lattice ECC for NAND Flash Memory

Tom Parnell, CTO
Siglead Europe
ECC for NAND Flash Memory

• The challenges facing ECC for NAND are well understood

• As information density increases (e.g. sub 20-nm process), cells become less reliable and stronger ECC is needed to achieve performance

• We believe it is necessary to design ECC specifically to suit NAND flash memory rather than lifting directly from other storage tech. (e.g. HDD)

• Here we present a new ECC architecture based on a lattice structure that is optimized for NAND flash memory
## Lattice ECC – Technical Spec.

<table>
<thead>
<tr>
<th>ECC Type:</th>
<th>BCH</th>
<th>LDPC</th>
<th>LATTICE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Decoder Type</strong></td>
<td>Hard</td>
<td>Soft</td>
<td>Hard or Soft</td>
</tr>
<tr>
<td><strong>RAW BER</strong>(^1)</td>
<td>3x10(^{-3})</td>
<td>?</td>
<td>2x10(^{-2})</td>
</tr>
<tr>
<td><strong>uPER Eval.</strong></td>
<td>Easy</td>
<td>Hard</td>
<td>Easy</td>
</tr>
<tr>
<td><strong>Complexity</strong>(^2)</td>
<td>O(N log(N))</td>
<td>O(N)</td>
<td>O(N)</td>
</tr>
<tr>
<td><strong>Error Floor</strong></td>
<td>No</td>
<td>Yes</td>
<td><strong>Hard Mode</strong>: No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Soft Mode</strong>: lower than LDPC</td>
</tr>
</tbody>
</table>

\(^1\) - RAW BER required to achieve operational PER=10\(^{-15}\) over Gaussian MLC channel with overall coding rate=0.85

\(^2\) – Complexity in terms of code block length (there are of course other considerations for implementation e.g. number of BP iterations)
• MLC 25nm NAND
• 6000 random program/erase cycles (applied according to JEDEC standard)
• 10 years data retention time
• Close to 1 billion pages captured using SigNas II software + FPGA

Experiment matches theory closely down to very low uPER!
Gaussian MLC Channel

- X – programmed state
- Cell Voltage Levels
  - $V|X=11 \sim N(\mu_{11}, s_{11})$
  - $V|X=01 \sim N(\mu_{01}, s_{01})$
  - $V|X=00 \sim N(\mu_{00}, s_{00})$
  - $V|X=10 \sim N(\mu_{10}, s_{10})$

Repeated applications of NAND RR feature can produce soft-outputs that approach LLRs given by this model (or similar)

$$LLR_v = \log \left( \frac{0.5 \Pr(V|X = 10) + 0.5 \Pr(V|X = 11)}{0.5 \Pr(V|X = 00) + 0.5 \Pr(V|X = 01)} \right)$$

$$LLR_L = \log \left( \frac{0.5 \Pr(V|X = 01) + 0.5 \Pr(V|X = 11)}{0.5 \Pr(V|X = 00) + 0.5 \Pr(V|X = 10)} \right)$$
Demonstration – Hard Mode

- Code block length \( N = 8192 \)
- All schemes have coding rate \( R = 0.847 \)
- BCH is \( t = 97 \) bit correctable

Lattice ECC (hard mode) can achieve \( uPER = 10^{-15} \) with around 2x increase in RAW BER compared with BCH
Demonstration – Soft Mode

- Code block length $N=8192$
- All schemes have coding rate $R=0.847$
- BCH is $t=97$ bit correctable

Lattice ECC (soft mode) can achieve $u\text{PER}=10^{-15}$ with around $7\times$ increase in RAW BER compared with BCH.
Demonstration – Lifetime Gain

- MLC 25nm NAND
- 3000 random program/erase cycles
- Baked at 145°C at uniform intervals
- Arrhenius law ($E_A=1.1\text{eV}$) is used to calculate equivalent time at 55°C
- Code block length $N=8192+224(\text{ecc})$
- Both schemes have coding rate $R=0.97$

Lattice ECC lasts for 5x as long before uPER crosses $10^{-15}$ threshold
Demonstration – PE Cycle Gain

- MLC 25nm NAND
- Bake equivalent to 1.1 years at 55°C
- Code block length $N=8192+238(\text{ecc})$
- Both schemes have coding rate $R=0.97$

Lattice ECC can withstand **2x as many** PE cycles before uPER crosses $10^{-15}$ threshold
Conclusions

• A new ECC architecture based on lattice structure optimized for NAND flash memory
• Decoder has both algebraic structure and probabilistic elements
• No significant increase in complexity or R/W throughput
• Simple method for evaluating operational uPER

• Hard Mode:
  • 2x gain in RAW BER
  • 2x as many P/E cycles
  • 5x improvement in lifetime

• Soft Mode:
  • 7x gain in RAW BER
  • Technical details of algorithm will be revealed once patent process is completed (or under NDA)