19nm 112.8mm² 64Gb Multi-level Flash Memory with 400Mb/s/pin 1.8V Toggle Mode Interface

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Outline

- Introduction to 19nm 64 Gbit MLC NAND (400 Mb/s/pin interface)
- Chip Architecture for Small Die Size
- MLC Programs Techniques
- New Features (Read-Latency Reduction)
- Summary of Key Features
- Conclusion
Outline

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Since first 160nm 1Gb MLC was commercially introduced in 2001, Memory Density has expanded by over 100 times.
Comparisons of first 1Gb MLC and latest 64Gb MLC

<table>
<thead>
<tr>
<th></th>
<th>160nm</th>
<th>one-ninth</th>
<th>19nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>1Gb</td>
<td>64 times</td>
<td>64Gb</td>
</tr>
<tr>
<td><strong>Die Size</strong></td>
<td>137mm$^2$</td>
<td></td>
<td>112.8mm$^2$</td>
</tr>
<tr>
<td><strong>Mb/mm$^2$</strong></td>
<td>7.5</td>
<td>80 times</td>
<td>581</td>
</tr>
<tr>
<td><strong>Architecture</strong></td>
<td>Conventional Even / Odd</td>
<td>All-Bit-Line(ABL)</td>
<td></td>
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<tr>
<td><strong>SA configuration</strong></td>
<td>Both Sided</td>
<td></td>
<td>Single Sided</td>
</tr>
<tr>
<td><strong>Program unit</strong></td>
<td>2kB (= 512B x 4Plane)</td>
<td>8 times</td>
<td>16kB (=16kB x 1Plane)</td>
</tr>
<tr>
<td><strong>tProg</strong></td>
<td>1.1ms</td>
<td></td>
<td>1.1ms</td>
</tr>
<tr>
<td><strong>Prog. Perform.</strong></td>
<td>1.9MB/s</td>
<td>8 times</td>
<td>15MB/s</td>
</tr>
<tr>
<td><strong>Burst Cycle Time</strong></td>
<td>20Mb/s/pin(50ns)</td>
<td>20 times</td>
<td>400Mb/s/pin(2.5ns)</td>
</tr>
<tr>
<td><strong>Year</strong></td>
<td>2001</td>
<td></td>
<td>2011</td>
</tr>
</tbody>
</table>
Comparisons of 3bit /cell and 2bit /cell

- Two different directions (3bit/cell and 2bit/cell)
  - 3bit/cell enables highest Mb/mm²
  - 2bit/cell offers better performance and reliability

Note: D# = # bits per cell
Outline

- Introduction

- **Chip Architecture for Small Die Size**
  - Single-Array Configuration
  - One Sided All-Bit-Line (ABL) Architecture
  - High Speed Toggle Mode Interface

- MLC Programs Techniques

- New Features (Read-Latency Reduction)

- Summary of Key Features

- Conclusion
Single Array Configuration

Conventional Evne / Odd Architecture

- 32Gb Cell Array
- 16kB-cells
- 8kB-Page

2-Plane array configuration

All-Bit-Line (ABL) Architecture

- 64Gb Cell Array
- 16kB-cells

Single array configuration ⇒ Small Die size
Two-Sided Sense Amp Architecture

- Half of SAs are placed on each side of the array due to complexity of SA layout.
One Sided ABL Architecture

- Same Metal pitch in SA as BL pitch
- Spacer patterning process

Conventional Two-sided SA

This work One-sided SA
Die Size Reduction

117.3mm² (100%) → 112.8mm² (94%) (fit into uSD)

- Peripheral Circuits: -25%
- Sense Amplifier: -30%
- Row Decoder
- Cell Array

Conventional Two-sided SA

This work One-sided SA
High Speed Toggle Mode Interface

Conventional
Two-sided sense amplifier

- Minimized signal delays
- Lower power consumption

This work
One-sided sense amplifier
400Mb/s/pin @ 1.8V high-speed toggle mode interface is achieved!
Introduction

Chip Architecture for Small Die Size

MLC Program Techniques
  • Bit-Line Bias Acceleration (BLBA)
  • BC-States-First Program Algorithm

New Features (Read-Latency Reduction)

Summary of Key Features

Conclusion
Bit-Line (BL) RC

24nm 64Gb D2

Bit-Line ~ 65,000 cells

19nm 64Gb D2

Bit-Line ~ 130,000 cells

- Cells connecting to one Bit-Line is doubled
  
  \[ \Rightarrow \text{Larger Bit-Line (BL) RC} \]
Bit-Line Bias Acceleration (BLBA)

- **Acceleration Period**
  - Bit-Line Voltage:
    - "VBL+Vth"
    - "VBL"
  - Time:
    - "ON"
    - "OFF"

- **Sense Period**
  - Bit-Line Voltage:
    - "VBL+Vth"
    - "VBL+Vth"
  - Time:
    - "ON"
    - "OFF"

→ Bit-Line pre-charge time is reduced by 20%
Conventional-Program Algorithm

State “b” and “c” Programming voltage is “high”
BC-States-First Program Algorithm

Program pulse
WL Voltage
state “c” verify
State “b” verify
State “a” verify

→ “Program disturbs” and “cell-to-cell coupling effect” are suppressed
→ Bigger incremental step size can be applied
MLC Program Improvement

- High program throughput with high reliability

- All-Bit-Line architecture (ABL)
- Bit-Line Bias Acceleration (BLBA) (6%)
- BC-states-first program algorithm (8%)
- Air Gap technology reduces FG coupling effect and word line (WL) RC (10%)

Program throughput: 15MB/s (16kB)
tProg: 1.1ms
Introduction
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Program-Suspend Function

- Operation
  - Prog. Command
  - Read Command

- Cache Ready/Busy
  - Cache Busy

- True Ready/Busy
  - True Busy Prog.

- Internal operation (WL voltage)
  - Prog
  - P.V
  - Prog
  - P.V
  - Prog
  - P.V

- Any page within any block can be read
Read data shifted out while program resumes
- Same sequence as at Reset command.
- Program operation as well as read operation is available without any restrictions on address input
Erase-Suspend Function

- Read data can be shifted out upon resume of erase sequence.
Read latency at program/erase is improved to 50us, which is comparable to normal read latency (~40us).

- Program-suspend function
- Erase-suspend function
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Summary of Key Features

- Density: 64Gb, 2-bit/cell
- One sided ABL architecture
- Organization
  - 16kB / Page
  - 2 Pages / WL
  - Single-array configuration
- Program Throughput: 15MB/s
- Burst Cycle Time: 400Mb/s/pin Toggle mode @1.8V
- Power Supply: 2.7V to 3.6V
- Technology: 3-Metal 19nm CMOS
- DieSize: 112.8mm²
Conclusion

- For the first time, a 112.8mm² 64Gb Multi-level (2bits/cell) NAND flash memory is developed
  - 19nm CMOS technology
  - Single Array configuration
  - One sided All.Bit.Line

- 400Mb/s/pin 1.8V high speed Toggle Mode interface

- 15MB/s programing throughput with high reliability
  - Bit-Line Bias Acceleration(BLBA)
  - “BC” states-First program algorithm

- Read latency is improved by Program-Suspend and Erase-Suspend functions
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