Flash Controller Solutions in Programmable Technology

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Overview

- What is a PLD?
- Programmable Technology for Flash Controllers
- Example Applications
- Notable Emerging Memory Types
A programmable logic device (PLD) is a type of semiconductor.

Most semiconductors can be programmed only once to perform a specific function.

PLDs are reprogrammable—functions can be changed or enhanced during development or after manufacturing.

**Flexibility Makes PLDs Lower Risk and Faster to Design Than Other Types of Semiconductors**
PLD Tipping Point vs. ASICs

Source: Altera; data applies to new design starts.
Enabling Technology-
Programmable Logic Devices

• Design Logic support
  - Increasing densities to support system on chip (SOC) programmability
• Increased Computational Performance
• Reduced Power
  - Intelligent power management
  - Hardened IP blocks
• High Speed Serial Interface Support
  - Embedded Transceivers
Cost Reduction by Integration

Before

After

3 Gbps

Device(s)

FPGA

Multiport Memory Controller

400 Mbps

Memory

Device(s)

FPGA

Multiport Memory Controller

5 Gbps

Device(s)

CPU

Device(s)

Soft IP

Hard IP
Balancing a FPGA Family by Process Technology

TSMC’s 28-nm Low-Performance (LP) Process and Design Optimizations

- The optimal choice for addressing today’s power- and cost-constrained applications
- Lowest absolute power

TSMC’s 28-nm High-Performance (HP) Process and Design Optimizations

- Highest bandwidth
- 28G transceivers at 200 mW
- Lowest power in high-performance systems
A Complete Solutions Portfolio

- **MAX Series**: Lowest Cost, Lowest Power CPLDs
- **Cyclone Series**: Lowest Cost, Lowest Power FPGA
- **Arria Series**: Cost- and Power-Optimized FPGA
- **Stratix Series**: Highest Bandwidth FPGA
- **HardCopy Series**: Lowest Risk, Lowest Total Cost ASICs

**Nios II**
- MIPS Technology
- Embedded Soft Processors

**ARM**
- Intellectual Property (IP)

**Quartus II**
- Design Software

**Development Kits**
PLD’s Have Evolved!

The Lab

Prototyping
1-250 units

The Data Center

Production
10ku-1Mu
# Data Center Applications - Servers

<table>
<thead>
<tr>
<th>Application</th>
<th>Usage Examples</th>
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</thead>
<tbody>
<tr>
<td>Flash SSD</td>
<td>PCIe to ONFI bridging, Flash Control</td>
</tr>
<tr>
<td>Acceleration</td>
<td>Algorithm acceleration for vertical markets</td>
</tr>
<tr>
<td>Bridge Plus</td>
<td>Interface bridging with IP function, e.g. compression and encryption, Dedupe</td>
</tr>
<tr>
<td>I/O Virtualization (10GbE and PCIe)</td>
<td>ASIC alternative; low cost with flexibility</td>
</tr>
<tr>
<td>Co-ASIC</td>
<td>Features enhancement</td>
</tr>
<tr>
<td>Management (BMC, KVM)</td>
<td>IP Flexibility supported with low power</td>
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</table>
### Data Center Applications - Storage

<table>
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<tr>
<th>Application</th>
<th>Usage Examples</th>
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<tbody>
<tr>
<td>Flash Cache/SSD</td>
<td>ONFI bridging and RAID adaptor NV DIMM backup, RAID for Flash</td>
</tr>
<tr>
<td></td>
<td>Memory BackUp/Restore</td>
</tr>
<tr>
<td>RAID Bridging</td>
<td>PCIe Gen 3 x8 best of class signal integrity</td>
</tr>
<tr>
<td>Bridge Plus</td>
<td>Interface bridging with IP function</td>
</tr>
<tr>
<td>ASIC Replacement</td>
<td>Lower cost development with flexibility</td>
</tr>
<tr>
<td></td>
<td>Tape</td>
</tr>
</tbody>
</table>
Flash Controller Applications
Flash Controller Requirements

- Uncertainty Favors PLDs for Flash Control Solutions
- Flash Challenges Continue
  - Data loss, slow writes, wear leveling, write amplification, RAID
- Many Performance Options
  - Write back cache, queuing, interleaving, striping, over provisioning
- Many Flash Cache Opportunities
  - Server, blade and appliance
Flash Controller Design Challenges

- Emerging memory types
  - ONFI 3.0, Toggle Mode 2.0
  - PCM, MRAM
  - DDR4

- Controller Performance Options
  - Write back cache, queuing, interleaving, striping

- ECC levels
  - BCH encryption

- Data transfer interface support
  - PCI Express, SAS/SATA, FC, IB
<table>
<thead>
<tr>
<th>IP</th>
<th>Sources</th>
<th>IO</th>
<th>Speed</th>
<th>Logic Density</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ONFI 3.0</td>
<td>SLS, Cadence</td>
<td>40 pins/ch</td>
<td>400 MTps</td>
<td>5KLE/ch</td>
<td>NAND flash control, wear leveling, garbage collection</td>
</tr>
<tr>
<td>Toggle</td>
<td>SLS, Cadence</td>
<td>40 pins/ch</td>
<td>400 MTps</td>
<td>5KLE</td>
<td>Same</td>
</tr>
<tr>
<td>Mode 2.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR3</td>
<td>Altera</td>
<td>72 bit</td>
<td>1066 MHz</td>
<td>10KLE</td>
<td>Flash control modes available for NVDIMM</td>
</tr>
<tr>
<td>PCM</td>
<td>Micron</td>
<td></td>
<td></td>
<td>5KLE</td>
<td>PCM- Pending production $</td>
</tr>
<tr>
<td>MRAM</td>
<td>Everspin</td>
<td></td>
<td></td>
<td>5KLE</td>
<td>MRAM- Persistent memory controller (Altera based)</td>
</tr>
<tr>
<td>PCIe</td>
<td>Altera</td>
<td>G3x8</td>
<td>64Gbps</td>
<td>HIP</td>
<td>Flash Cache</td>
</tr>
</tbody>
</table>
PCI Express Support

Hardened IP (HIP) Advantages
- Resource savings of 8K to 30K logic elements (LEs) per hard IP instance, depending on the initial core configuration mode
- Embedded memory buffers included in the hard IP
- Pre-verified, protocol-compliant complex IP
- Shorter design and compile times with timing closed block
- Substantial power savings relative to a soft IP core with equivalent functionality

PCIe Mode | Thruput (GT/s per lane) | Production
---|---|---
Gen 2 | 2.5 | Now
Gen 3 | 5.0 | Now
Gen 4 | 8.0 | 2016

Note:
1. LMI: Local Management Interface
2. DPRIO: Dynamic Partial Reconfigurable Input/Output
- Flash Controllers can manage SAS/SATA SSD interfaces
- 12Gbps SAS support required for enterprise drives
- FPGA transceivers need to support electrical performance and OOB signaling
*Intelliprop Hydra* can provide 4X the capacity and up to 4X the performance of a single drive.

**Applications**

- SSD manufacturers with a need to build larger drives (1TB, 2TB, 4TB)
- Applications requiring stable read/write bandwidth
- Enterprise systems requiring high IOPS and bandwidth
- Host systems writing large amounts of “raw” data
- Systems where economical controllers can be used while still achieving performance of “enterprise” class controllers
**Test Conditions**
- Non-compressible data
- Testing done using IOMETER 2010
- Testing with HYDRA in 4 port configuration using 32-bit DRAM
- 4kB page size flash
- Host PC: Intel Core i7-3770K Ivy Bridge 3.5GHz
FPGA RAID Controller for Flash Arrays

- 10+TB plus of Flash Storage
- FPGA Applications
  - Flash Control
  - RAID
  - Data Transfer
PLD Violin Product Portfolio

**V3000: Performance Apps**

- Any SAN/PCle
- High Reliability
- Low entry cost
- 5TB-20TB per 3U
- 100K – 200K IOPS

**Technologies**

- Block Storage with full performance and flexible LUN management
- Array management software with Web, CLI, Email and XML & Clustering
- Hardware Flash RAID with 4+1 efficiency

**V6000: Primary Flash Storage**

- HA in box
- High bandwidth
- Integrated SAN
- 6-32TB per 3U
- 200K-1M IOPS

**Technologies**

- Violin Intelligent Memory Modules (VIMMs) with distributed grooming
High Availability
No Single-Point-of-Failure and Hot Swap Everything

- Memory Gateway x2
- Network Interface x4
- Array Controller x2
- VIMMs x24/44/64
- vRAID Controller x4
- Power Controller x2
- Power Supplies x2
- Fans 3x2
Flash Cache
PCIe or Appliance

**Benefits**
- High performance for cache
  - Better bandwidth vs SSD
    - PCIe up to 5X
- Lower power than DRAM
- Less space than disk based
- Hardcopy (structured ASIC) path

**Solution**
- Altera
  - ONFI 2.0 & Toggle Mode cards
  - ONFI 3.0 daughtercard (3Q12)
  - ONFI 3.0 App Note (3Q12)
- Partner
  - Denali/Cadence IP
  - SLS for single channel controller
Flash Cache Controllers

Denali Multi Channel Controller
• Single to multi Flash channel capability
• Basic NAND development platform
• Provides High Speed ONFI & Toggle NAND PHY
• ECC of 8 and 15 bits of error correction

Third Party Single Channel Controllers
Data Integrity - The Green Approach

Battery Backed Data Recovery

Add-on modules that protect against data loss in the event of a server or power failure by providing emergency power to the cache memory. When power is restored, the data not yet written to the hard drives can be retrieved from cache memory.

Super Capacitor Based Alternative

<table>
<thead>
<tr>
<th>Benefit</th>
<th>Battery Power Source</th>
<th>Super Cap Power Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Less Cost</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Lower Power</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Smaller Footprint</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Field service required</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Permanent backup</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
NVDIMM Controller Architecture

- Processor
- DDR
- FPGA (Cyclone)
- DIMM
- FET bank
- Power failure switch
- I2C
- DDR ctrl with tri-state
- Power regulation
- Flash 1 or 2 SD Cards or BGA

- Can be
  - Buffered
  - Un-buffered
  - Registered

- On power failure, these FETs switch out the processor signals

- 400MHz / 800MB tested

- 5 or 9

- To super-cap bank
Hybrid RAID System
- Persistent DRAM and Flash Caches
Hybrid RAID System - PCIe Switch Centric

Network Side

FC HBA

PCI-e

Persistent DRAM

PCI-e or CPU System Bus

PCI-e

Dual Controller

Disk Side

FC HBA

SATA

SAS

ASSPs

FPGA Controller

Flash Cache

Dedupe/Encrypt
Programmable Logic Devices (PLDs) are a well suited technology for emerging flash memory controller requirements.

- Multiple memory types
- BCH enhancements
- Emerging technologies (MRAM)
- High Speed Interface Requirements (PCIe, SAS)

Visit the Altera Exhibit Booth to Learn More!