3D-IC is Now Real: Wide-IO is Driving 3D-IC TSV

Samta Bansal, Cadence
Flash Memory Summit
August, 2012
What the fuss is all about …

* Source: ECN Magazine March 2011

Samsung Wide-IO Memory for Mobile Products - A Deeper Look

<table>
<thead>
<tr>
<th></th>
<th>Conventional 3D Package (FC-PoP) with LPDDR2</th>
<th>TSV-SiP with Wide IO memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory I/O Power Consumption</td>
<td>176 mW</td>
<td>44 mW</td>
</tr>
</tbody>
</table>

Comparision of package performance: wire-bonding PoP vs wide IO interface with TSV (Courtesy of Samsung)

Faster, Denser, Low-power Chips Using 3D-IC TSVs

Micron develops “Hyper Memory Cube” 3DIC technology

* Source: Tech Spot Feb 2011 & Flash Memory Summit August 2011
CPU to DRAM
Existing inter-die connection methods

Parallel Connection across a PCB
- Most common CPU/SoC-to-DRAM connection today
- Well understood and extensible
- Many pins required for high bandwidth
  - ~60 signal pins for a 32-bit LPDDR2 interface (2012 low-mid range smartphone)
  - ~120 signal pins for a 2-channel LPDDR2 interface (2012 mid-high end smartphone)
  - ~300 signal pins for a 3-channel 64-bit DDR3 interface (2012 PC)

Serial Connection Across a PCB
- Fewer pins than parallel connection
- Common for PCIe and other SerDes-based standards
- Can provide data transfer over longer physical distances if needed
- Potential latency and power considerations
- Not commonly used for DRAM at present; future solution?

Pin Count, Power, Latency Concerns?
New inter-die connection method - TSV
What is Wide-IO DRAM?

**Current Standard**
- 4 128-bit channels
- Total 512bits to DRAM
- 200MHz SDR
- 100Gbit/s bandwidth

**Possible Future Standard**
- 4-8 64-128-bit channels
- 256-512bits to DRAM
- DDR Interface
- 200-400Gbit/s bandwidth
- 2Tbit/s bandwidth

**Possible Future Standard**
- 4 128-bit channels
- Total 512bits to DRAM
- 1066MHz DDR (2133MT/s)
- 1Tbit/s bandwidth

Possible time of introduction
What is HMC Architecture?

Abstracted Memory Management

Memory Vaults Versus DRAM Arrays
Logic Base Controller

Through-Silicon Via (TSV) Assembly

Innovative Design & Process Flow
Advanced Package Assembly

Increased Bandwidth,
Power Efficiency,
Smaller Size, Scalability
& Reduced Latency
Why do you need Wide-IO DRAM?

Bandwidth Requirements of Future Mobile Devices

<table>
<thead>
<tr>
<th>Solutions</th>
<th>LPDDR2 533 MHz</th>
<th>LPDDR3 800 MHz</th>
<th>WideIO 200 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single Channel</td>
<td>Dual Channel</td>
<td>Single Channel</td>
</tr>
<tr>
<td>Density (2014)</td>
<td>2x4 Gb</td>
<td>4x4 Gb</td>
<td>2x8 Gb</td>
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<tr>
<td>Bandwidth</td>
<td>4.25 GBy/s</td>
<td>8.5 GBy/s</td>
<td>6.4 GBy/s</td>
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<tr>
<td>Power (burst read)</td>
<td>330 mW</td>
<td>660 mW</td>
<td>430 mW</td>
</tr>
<tr>
<td>Power / Bandwidth</td>
<td>78 mW/GByps</td>
<td>67 mW/GByps</td>
<td>43 mW/GByps</td>
</tr>
<tr>
<td>Cost (2014)</td>
<td>N/R</td>
<td>1</td>
<td>N/R</td>
</tr>
</tbody>
</table>

WideIO provides 2x power efficiency compared to LPDDR2/3
- The initial JEDEC proposal is providing 12.8 GByte/s bandwidth. Increasing DRAM frequency to 266 MHz and implementing dual data rate transfers will provide eventually more than 34 GBytes/s.
Why Wide-IO is driving TSV

DRAM is the ideal candidate to drive TSV technology

• Usually manufactured on a non-logic process
• Requires high bandwidth connection between CPU and DRAM
• Uneconomic or impossible to place large capacity (Gbits) of DRAM on same die as CPU
• Low power connection between dies desirable
• Possibility of different memory configurations using the same CPU die
## Cadence Wide-IO DRAM controller

<table>
<thead>
<tr>
<th>Challenges</th>
<th>Solutions</th>
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<tr>
<td>Merge existing and new technology</td>
<td>• Start with extensible, high performance, low-power base architecture (Supports DDR1, DDR2, DDR3, LPDDR1, LPDDR2 and now DDR4)</td>
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<td>• Re-add SDR support</td>
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<td>• Add new Wide IO feature support</td>
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<td>• Create DFI extensions for Controller-PHY connection</td>
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<td>New testing requirements</td>
<td>• Extend BIST engine to test for new classes of error</td>
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<tr>
<td>Verification</td>
<td>• Create memory model of Wide-IO device in Cadence VIP tools</td>
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<td>• Extend existing configurable verification environment for Wide IO</td>
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Real chip, real examples

**Wioming test chip program**

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<th>Same SoC addressing several schemes of 3D integration</th>
<th>Proof of concept for:</th>
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<tr>
<td></td>
<td>Technology</td>
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<td><strong>Wide IO demonstrator:</strong> DRAM on Wioming</td>
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<td>High speed CMOS techno 70mm² 2000 TSVs 1000 bumps 500 balls</td>
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Cadence silicon-proven 3D-IC solution
Plan → implement → test → verify

• Allows heterogeneous integration to offer power, performance in smallest form factor

• **Cadence is technology leader providing complete and integrated 3D-IC solution**
  – Plan->implement->test->verify
  – 1st to market wide I/O memory controller

• **Developed in close partnership for past 5 years with leading foundries and customers**

• **Multiple 3D-IC tapeouts**
  – Multiple testchip experience: Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  – Production design tapeout in mid-2010
Several challenges with TSV technology

- Manufacturing Wide-IO DRAM and assembly
  - Test memory wafer after production using FC bumps
  - Thin the wafer to ~50-100um thickness
  - Form TSVs and fill with metal: Requires elevated temperatures
  - No opportunity to test here
    - Backside metal bump pitch too fine for most tester heads
  - Handle dies while avoiding mechanical damage
    - They are now the approximate aspect ratio of a postage stamp
  - Attach dies (and interposers, if present) together
  - Does it still work?

- Thermal Issues
  - Where does the heat go?

- Ecosystem Issues:
  - How many parties involved in stack production?
  - How are responsibilities divided?
  - How are liabilities divided?
Conclusion

• Wide-IO and TSV are real
• Cadence believes that Wide-IO DRAM is the technology that will drive adoption of TSV
• Cadence stands ready with EDA tools and IP to enable your TSV designs with real experiences and partnerships with ~8 testchips and 1 production chip already completed.