Phase Change Memory Landscape

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### Phase Change Memory Values

<table>
<thead>
<tr>
<th>Attribute</th>
<th>PCM</th>
<th>NOR</th>
<th>NAND</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Volatile</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Granularity</td>
<td>Small/ Byte</td>
<td>Large</td>
<td>Large</td>
<td>Small/ Byte</td>
</tr>
<tr>
<td>Erase</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Software</td>
<td>Easy</td>
<td>Moderate</td>
<td>Hard</td>
<td>Easy</td>
</tr>
<tr>
<td>Power</td>
<td>~Flash</td>
<td>~Flash</td>
<td>~Flash</td>
<td>High (SB)</td>
</tr>
<tr>
<td>Write Bandwidth</td>
<td>~100 MB/ s</td>
<td>~1 MB/ s</td>
<td>~10 MB/ s</td>
<td>~1000 MB/ s</td>
</tr>
<tr>
<td>Read Latency</td>
<td>50 - 100 ns</td>
<td>70-100 ns</td>
<td>15 - 50 us</td>
<td>20 - 80 ns</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^6+$</td>
<td>$10^5$</td>
<td>$10^{4-5}$</td>
<td>Unlimited</td>
</tr>
</tbody>
</table>

PCM provides an new set of features combining components of NVM with DRAM
Phase Change Memory History

January 1955: Kolomiets/Gorunova - semiconducting properties of chalcogenide glasses
September 1966: Stanford Ovshinsky files first patent on phase change technology
September 1970: 256b PCM memory demonstrated – Gordon Moore
June 1999: Ovonyx joint venture is formed to commercialize PRAM technology
February 2002: Intel demonstrates 4Mb test vehicle
August 2004: Samsung announces successful 64 Mbit PCM array
September 2005: Samsung announces successful 256 Mbit PCM array
July 2006: BAE Systems sells the first commercial PCM, Radiation Hard 512Kx8 chip
September 2006: Samsung announces 512 Mbit PRAM device
October 2006: Intel and STMicroelectronics show a 128 Mbit PCM chip
February 2008: Intel and STMicroelectronics announce four-state MLC PCM
December 2008: Numonyx announces production 128 Mbit PCM device
September 2009: Samsung announces production start of 512 Mbit PCM device
October 2009: Intel and Numonyx announce an all thin film 3-D PCM device
December 2009: Numonyx announces 1 Gb PCM at 45 nm
April 2010: Numonyx releases Omneo PCM Series (P8P and P5Q), both in 90 nm
April 2010: Samsung releases 512Mbit PCM with 65 nm process, in Multi-Chip-Package
PCM Development Activities

- Scaling the existing architecture, providing the smallest cell size, following the lithography roadmap
- Introduction of Multi-Level-Cell exploiting the analog storage capability of PCM
- Exploration of new chalcogenide alloys which may open new application fields
- Exploitation of a true cross-point array which will allow vertical stacking of more than one memory layer