SSD Subsystem
Chip-to-Chip Interfaces

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Agenda

- SSD Architecture Overview
- SSD Interconnection
- Interface Design Parameters
- High-Speed Considerations
Micron SSDs

2.5-inch SSD

1.8-inch SSD

PCle SSD
SSD Density Is Growing

SSD Density by Segment (GB)

Source: iSuppli
SSD Subsystem Architecture

How to connect as many devices as possible without degrading performance and increasing system complexity
Micron 64GB 2.5-inch SSD
SSD System Design Tradeoffs

SSD system architecture must be optimized for:

- Performance (higher bandwidth and lowest latency)
- Lowest power
- Fewest pins
Loading Effect

When sharing a common bus, devices cannot drive the bus with the maximum data rate due to the increase in bus loading.
System Interconnect Figures of Merit

- Compare among different configurations and interfaces
- System figures of merit are the metric parameters—the merits depend on the system design trade-offs
- Focus on BW/pin, latency, and energy/bit
A storage memory subsystem can require as much as GBs of capacity:
- Connecting memory devices in parallel (system level)
- Stacking many devices in one package (package level)
- Trade-offs: parallelism, pins, power

Signal integrity analysis is needed
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Dr. Mostafa Abdulla has 20 years of research and development expertise in the electronics and communications industries. A senior member of IEEE, he contributed to the creation of JEDEC LPDDR2, eMMC, and UFS standards. Currently, Dr. Abdulla serves as a senior engineering manager for Micron Technology, focusing on the development of high-speed circuits and architectures for memory subsystems, including the emerging field of stacked memory subsystems. He earned B.S. and M.S. degrees in electronics and communication engineering from Ain Shams University, a Ph.D. degree in electrical engineering from North Carolina State University, and an MBA degree from Golden Gate University.