Emerging Challenges in NAND Flash Technology

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Presentation Agenda

- NAND Flash Market Overview
- Technology Scaling Trend & Forecast
- Technology Scaling Limitation & Hurdle
- Future Technology Development Direction
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Market Revenue Forecasting

Expect continuous NAND market growth; $29.1B in 2014

WW NAND Revenue Trend

[Source; WSTS2011]
Prospective Application Trend

Mobile, Tablet, SSD dominate NAND demand in 2011~2014

NAND Demand by Application

[Source; Hynix Marketing 2011]
General Market Requirement

- Low Cost
  - Bit growth

- High Performance
  - + Controller SW solution

- High Reliability
  - + Controller SW solution
Standard Interface Trend; **Performance**

- **2010**: ONFI 2.0, 133MB, Ver 4.0: 52MB, Ver 4.4: 104MB, Ver 4.5: 200MB
- **2011~2012**: ONFI 2.2/Toggle 1.0, 400MB, Ver 1.0: 2.9GB (360MB), Ver 2.0: 5.9GB (720MB), Ver 3.0: 12GB (1.5GB)
- **2013**: ONFI 3.0/Toggle 1.5, 900MB, Ver 3.0: 3GB (360MB), Ver 4.0: 6GB (750MB), Ver 5.0: 12GB (1.5GB)
- **2014~2015**: ONFI 4.0/Toggle 2.0, 1.6GB, Ver 4.1: 2GB (600MB), Ver 5.0: 4GB (3GB), Ver 6.0: 8GB (3GB)

- **Serial Interfaces**
  - PCIe
  - USB
  - SD
  - DRAM

- **50MB/s, 100MB/s, 200MB/s, 400MB/s, 800MB/s, 1.6GB/s, 3.2GB/s, 6.4GB/s**
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Further Scaling Solution?

Conventional FG NAND cell has been scaled down over 18 years.

- 0.7um → 2Xnm (Cell size: ~1/2000)
- 1.5year/gen. (18 years / 12 gen.)
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Scaling Limitation of FG Cell

◆ **Physical Limitation;**
  ✓ Patterning
  ✓ Structure formation: FG, CG, IPD ...

◆ **Electrical Limitation;**
  ✓ Interference
  ✓ Capacitive coupling ratio
  ✓ No. of electron in FG
  ✓ Dielectric leakage
Cell Scaling Limitation; x-direction

- ASA-FG Advanced Self-Aligned Floating Gate

- BL Loading; → RC

- IPD & CG gap-fill; → Space

- Cell Current ∝ W → Width
Cell Scaling Limitation; y-direction

- WL Loading; → RC delay
- Cell S/D Punch; → Off leakage
- Interference; → Vt distribution
NAND Program Speed

- **Program Speed** = \( t \) (PROG + Verify) \( \times \) N
  - \( t_{\text{PROG}} \); unit program & verify time
  - N; no. of ISPP
WL & BL Loading Improvement

- **WL Loading**
  - Material; Poly- Si → CoSix → W
  - WL Space; Vertical Profile → Low-k dielectric → Air Gap

- **BL Loading**
  - Material; W → Al → Cu
  - BL Space; Vertical Profile → Low-k dielectric → Air Gap
No. of stored electrons in FG

\[ \Delta V_{th-max} = 3V \]

Flash Technology Node [nm]

Number of Electron per bit, [N]

Program Operation

CG (Positive)
ONO
Oxide

P- Well

NOR Flash Projection
(ITRS 2003)

IEDM Papers

NOR Flash Projection
(ITRS 2003)

1xnm 2ynm

\[ 1 \times nm \]

\[ 2 \times nm \]

\[ 100 \]

\[ 1000 \]

\[ 100 \]

\[ 10 \]

Flash Technology Node [nm]

Number of Electron per bit, [N]
Read Window Margin Solution

Vt Distribution Overlap due to:
- Process Variation
- Data Retention Shift
- FG-FG Interference

Controller Solution
- Smart Read Algorithm
- Strong ECC
Enhanced Solution Products

- **Hynix; E2NAND**
  
  [embedded-ECC]
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Planar FG with High-k IPD

◆ CG Gap-filling & Interference

❖ Thin FG structure with High-k IPD

✓ FG vertical scaling
3D Cell Structure Approach

- Stacked 3D with SONOS structure
- Stacked 3D with FG structure
- Si Pillar 3D with wafer bonding technology
# History of 3D NAND Flash

<table>
<thead>
<tr>
<th>~2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SONOS / TANOS</strong>&lt;br&gt;Stacked NAND IEDM 2006&lt;br&gt;Multi TFT IEDM2006&lt;br&gt;Si Pillar 3D NAND Semi. International 2007&lt;br&gt;S-SGT IEDM 2001</td>
<td><strong>TOSHIBA</strong>&lt;br&gt;BiCS VLSI Symp</td>
<td><strong>TOSHIBA</strong>&lt;br&gt;P-BiCS VLSI Symp</td>
<td><strong>SAMSUNG</strong>&lt;br&gt;TCAT VLSI Symp</td>
<td><strong>SAMSUNG</strong>&lt;br&gt;VG-NAND VLSI Symp</td>
<td><strong>SAMSUNG</strong>&lt;br&gt;VG TFT VLSI Symp&lt;br&gt;<strong>Hyundai</strong>&lt;br&gt;Hybrid 3D IMW</td>
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Stacked 3D NAND Flash Concept

3D NAND Cell string

DCT

DSL

WL

SSL

SCT

String 1
String 2
String 3
String 4

Block
Stacked 3D Cell Structures

**P-BiCS**

**TCAT**

[VLSI 2009 by Toshiba]

[VLSI 2009 by Samsung]
Stacked 3D Cell Structures

Hybrid Stacked 3D

3D Cell Structure with Horizontal Poly-Si Channel

[IMW 2011 by Hynix]
Dual CG - Surrounding 3D FG Cell

- New 3D Structure Concept with FG cell
- Surrounding FG is controlled by two control gates.

Single cell


[IEDM 2010 by Hynix]
Si Pillar 3D Structure

Si Pillar

Cell Strings

Peripheral Region

[Semi. International 2007 by BeSang Tech.]
## Future Technology Analysis

<table>
<thead>
<tr>
<th>Technology</th>
<th>Strong Points</th>
<th>Weak Points</th>
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</thead>
<tbody>
<tr>
<td>Planar FG</td>
<td>Friendly Structure</td>
<td>High-k Dielectric Stability</td>
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<tr>
<td>FG-3D</td>
<td>Reliability</td>
<td>Scaling Limitation</td>
</tr>
<tr>
<td></td>
<td>Small Interference</td>
<td>Stacking Limitation</td>
</tr>
<tr>
<td>Stacked 3D</td>
<td>Low Cost</td>
<td>New Materials</td>
</tr>
<tr>
<td></td>
<td>Small Interference</td>
<td>SONOS Reliability</td>
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<tr>
<td>Si Pillar</td>
<td>Approved Materials</td>
<td>Wafer Bonding Cost</td>
</tr>
<tr>
<td></td>
<td>Scalability</td>
<td>SONOS Reliability</td>
</tr>
</tbody>
</table>
What are Decision Points?

- Process
- Cost
- Production Yield
- Reliability
Who is Winner at Post 1x or 1y nm?
Somebody will find a solution.

Thank you!