Error Control Coding for MLC Flash Memories

Ying Y. Tai, Ph.D.

Cadence Design Systems, Inc.
ytai@cadence.com
August 19, 2010
The Challenges on Error Control Coding (ECC) for MLC Flash Memories

Performance Measures on ECC

Low-Density Parity-Check (LDPC) Codes Overview

Performance of LDPC Codes for MLC Flash Memories

Conclusions
Challenges on ECC for MLC Flash Memories

- MLC Flash Memory:
  - Multiple bits are stored in each memory cell
  - Storage density increases
  - Process geometry downscale
  - Worse reliability
ECC Trend for Flash Memories:

- Bit error rate (BER) requirement: $10^{-13} - 10^{-16}$
- Hamming codes for SLC flash memory
- BCH codes for MLC flash memory (codeword length increases from 512 to 1K to 2K bytes)
- What is the next?
  - Reed-Solomon (RS) codes?
  - Low-Density Parity-Check (LDPC) codes?
Performance Measures on ECC

- **Error Probability:**
  - Bit error rate (BER)
  - Symbol error rate (SER)
  - Word (frame or block) error rate
  - Error floor

- **Coding Gain**

- **Shannon Theoretical Limit**
Performance Measures on ECC

![Graph showing Coding Gain and Error Floors](image)
LDPC Codes Overview

A class of channel capacity approaching codes

Employed by various applications:

- IEEE 802.3 10G BASE-T Ethernet
- Digital Video Broadcasting – DVB-S2
- IEEE 802.16e WiMAX
- Long Term Evolution (LTE)
- Hard Disk Drive
- NASA LandSat Data Continuation Mission
- China Digital TV Standard – DTMB
What is LDPC Code?

- The null space of a sparse parity-check matrix $H$ over $\text{GF}(q)$, i.e. $c \cdot H^T = 0$

- Categories of LDPC codes:
  - Random LDPC codes
  - Structured LDPC codes

- Key properties on the performance:
  - Girth and cycle distribution
  - Degree distribution
  - Minimum distance
  - Trapping set structure
Quasi-Cyclic (QC) LDPC Codes

- The null space of an array of sparse circulants

Why QC-LDPC codes?
- Reduced complexity for encoding and decoding on hardware implementation
- Well-designed QC LDPC codes perform very well
  - Good BER
  - Large coding gain
  - Low error floor
  - Fast decoding convergence rate
- Systematic encoder
## Example: Cadence/Denali LDPC on AWGN Channel

<table>
<thead>
<tr>
<th>Comparison</th>
<th>Cadence/Denali LDPC Code</th>
<th>RS Code</th>
<th>BCH Code</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Size</strong></td>
<td>2K Bytes</td>
<td>2K Bytes</td>
<td>2K Bytes</td>
</tr>
<tr>
<td><strong>Overhead Size</strong></td>
<td>&lt; 5 %</td>
<td>&lt; 5 %</td>
<td>&lt; 5 %</td>
</tr>
<tr>
<td><strong>Error Correction Capability (t)</strong></td>
<td>N/A</td>
<td>35 Symbols</td>
<td>32 Bits</td>
</tr>
<tr>
<td><strong>Type</strong></td>
<td>Quasi-Cyclic</td>
<td>Cyclic</td>
<td>Cyclic</td>
</tr>
<tr>
<td><strong>Encoder Format</strong></td>
<td>Systematic</td>
<td>Systematic</td>
<td>Systematic</td>
</tr>
<tr>
<td><strong>Simulation (Emulation)</strong></td>
<td>C &amp; FPGA</td>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td><strong>Decoding Type</strong></td>
<td>Iterative Belief Propagation</td>
<td>Algebraic Decoding</td>
<td>Algebraic Decoding</td>
</tr>
<tr>
<td><strong>Transmission</strong></td>
<td>BPSK</td>
<td>BPSK</td>
<td>BPSK</td>
</tr>
<tr>
<td><strong>Channel</strong></td>
<td>AWGN</td>
<td>AWGN</td>
<td>AWGN</td>
</tr>
</tbody>
</table>
Example: Cadence/Denali LDPC on AWGN Channel

![Graph showing Bit Error Rate (BER) vs. E/N0 (dB)]
### MLC Flash Memories

<table>
<thead>
<tr>
<th>Level</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean (V)</td>
<td>6.50</td>
<td>4.55</td>
<td>3.25</td>
<td>0.00</td>
</tr>
<tr>
<td>Deviation (V)</td>
<td>$2\sigma$</td>
<td>$\sigma$</td>
<td>$\sigma$</td>
<td>$4\sigma$</td>
</tr>
<tr>
<td>Direct Mapping</td>
<td>00</td>
<td>01</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>Gray Mapping</td>
<td>01</td>
<td>11</td>
<td>10</td>
<td>00</td>
</tr>
</tbody>
</table>

The diagram illustrates the probability density function of cell threshold voltages for different mapping techniques. The table provides the mean and deviation values for each level.
Performance of LDPC on MLC Flash Memories (2 Bits / Cell)
Performance of LDPC on MLC Flash Memories (3 Bits / Cell)
Performance of LDPC on MLC Flash Memories (4 Bits / Cell)
Performance Comparison on MLC Flash Memories

<table>
<thead>
<tr>
<th></th>
<th>2 Bits / Cell</th>
<th>3 Bits / Cell</th>
<th>4 Bits / Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDPC vs RS</td>
<td>1.55 dB</td>
<td>1.67 dB</td>
<td>1.85 dB</td>
</tr>
<tr>
<td>LDPC vs BCH</td>
<td>1.80 dB</td>
<td>2.00 dB</td>
<td>2.20 dB</td>
</tr>
<tr>
<td>RS vs BCH</td>
<td>0.25 dB</td>
<td>0.33 dB</td>
<td>0.35 dB</td>
</tr>
</tbody>
</table>
Cadence/Denali NAND Controller w PHY Support
Conclusions

- Well-designed LDPC codes have good error performance and low error floor for MLC flash memories.
- QC-LDPC codes have advantages on implementation complexity for encoder and decoder.
- Gray mapping leads to extra coding gain.
- Cadence/Denali NAND Flash IP Solution provides the most advanced ECC technologies for memory systems.
References