The New EZ NAND in ONFi v2.3

Paul Lassa
Systems Architecture
SanDisk
paul.lassa@sandisk.com
Outline

- ONFi Overview
- Ultimate Challenge…
- What is EZ NAND?
  - Flash Memory Management vs. Device Management
  - Raw NAND vs. BA vs. EZ NAND
  - Technology-Dependent boundary
- ONFi 2.3 / EZ NAND - Minimal Changes
ONFi Workgroup Overview & Results

- ONFi continues to deliver **innovation & interoperability** enabling faster NAND adoption and **increasing performance**

<table>
<thead>
<tr>
<th>Spec Version</th>
<th>2H ‘06</th>
<th>1H ‘07</th>
<th>2H ‘07</th>
<th>1H ‘08</th>
<th>2H ‘08</th>
<th>1H ‘09</th>
<th>2H ‘09</th>
<th>1H ‘10</th>
<th>2H ‘10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Major Revisions</td>
<td>ONFi 1.0: Standard electrical &amp; protocol interface, including base command set</td>
<td>ONFi 2.0: Defined a high speed DDR i/f, tripling the traditional NAND bus speed in common use</td>
<td>ONFi 2.1: Additional features and support for bus speeds up to 200 MB/s</td>
<td>ONFi 2.2: EZ NAND / ONFi 2.3: Enabled ECC / management offload option</td>
<td>ONFi 3.0: Scaled high speed DDR i/f to 400 MT/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speed</td>
<td>50 MB/s</td>
<td>133 MB/s</td>
<td>200 MB/s</td>
<td>400 MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industry</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>ONFi – JEDEC Collaboration</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Slide provided by ADH – Intel / ONFi
Ultimate Challenge – The Super Controller

Super Host Controller
(Universal ECC Engine and Flash Device Management)

Host I/F to PC/Server:
(SATA, SAS, PCIe, XYZ...)

ONFi = Host to Flash I/F

Flash Vendor A
5x nm 3x nm 2x nm
SLC  SLC  SLC
MLC  MLC  MLC
8LC  8LC  8LC

Flash Vendor B
5x nm 3x nm 2x nm
SLC  SLC  SLC
MLC  MLC  MLC
8LC  8LC  8LC

Flash Vendor C
5x nm 3x nm 2x nm
SLC  SLC  SLC
MLC  MLC  MLC
8LC  8LC  8LC

Flash Vendor D
5x nm 3x nm 2x nm
SLC  SLC  SLC
MLC  MLC  MLC
8LC  8LC  8LC

8/19/10
Ultimate Challenge – The Super Controller

EZ NAND provides a solution for coping with the need for increasingly sophisticated ECC and Device management schemes that are carefully customized to particular vendor’s NAND devices.

In an ideal world, we could have a single Universal Host controller that optimally utilizes all the flavors of NAND that have evolved over the past 10 years, and extending out for the next 5-10 years, handling ECC and all the Device management tricks.

We know too well that this is not achievable.

The next best thing, which I’ll show today, is that we can offer a standard partitioning that allows the industry players to each handle what they do best.
Version 2.3 (planned release) Aug. 2010 – Main feature: **EZ NAND** function

- Areas of change:
  - Parameter Page: feature registers
  - ECC Off-Load
  - Read Retry
  - Corrected Copy
  - Status Register
  - Signal name standardization and “multi-plane” reference
  - Parametric extensions

* Backwards compatible to ONFi v2.2
**EZ** (ECC Zero) **NAND** – a NAND device / module that requires no ECC correction by the Host (ECC is handled internally to NAND package)

And **EZ NAND** is **Easy** to implement and support!

- Goal of EZ NAND is to create a packaged NAND that “hides” the technology dependent portions of NAND management.

- Simple ASIC stacked within a NAND package performs NAND device management functionality that is lithography specific (such as ECC and error correction), while retaining raw NAND protocol infrastructure.

- EZ NAND delivers an ECC offloaded solution with minimal command and/or protocol changes. The device **parameter page** specifies if EZ NAND is supported.
Some definitions / terminology …

- **Technology Independent components**
  - **Flash Translation Layer (FTL)** – mapping from Host bus (SATA, PCI, etc.) to Flash blocks, planes, pages
  - **Flash Memory Management (FMM)** - caching, garbage collection, storage optimization

- **Technology Dependent components**
  - **Flash Device Management (FDM)**
    - Examples:
      - ECC, Soft-error recovery, Wear Leveling, Scrubbing
    - Variations between:
      - **Generations** (lithography – 5x, 3x, 2x, … nm)
      - **Vendors**
      - **Bits/cell** – SLC, MLC, 3+ bits/cell
  - EZ NAND parts may be offered with:
    - Different performance / endurance / quality specs

➔ Technology Dependent issues becoming more significant and varied
1. **Standard ONFI / Raw NAND** – stand-alone Host Controller – Host performs all Flash control functions

   **Host Controller**
   (Flash Memory Management, ECC, Flash Device Management)

   **ONFi Channel**
   
   **Tightly coupled – difficult to interchange**

   **NAND Flash**

2. **BA (Block Abstraction)** – BA Flash controller frees Host from FMM and FDM, but …

   **Host Controller**
   (Driver only)

   **BA Flash Controller**
   (Flash Memory Management, ECC, Flash Device Management)

   **Limited Host control**

   **limited performance / optimization**

8/19/10
3. **EZ NAND** – Host retains Memory Management function, EZ NAND controller handles Technology-Dependent Flash Device Management.

**Goal:** Separate **Technology Independent** and **Technology Dependent**

- **Host Controller** (Flash Memory Management)
- **EZ NAND Controller** (ECC, Flash Device Management)
- **NAND Flash**

Optimized per Application! Optimized per NAND type!

**Benefits:**
- Host Controller works with **multiple types**, generations (and various performance points) of Flash
- Memory Management remains in Host for best optimization **per application**
EZ NAND Module – Technology-Dependent Operations Off-Load

Technology-Independent

- Flash Translation Layer
  - Mapping Host LBA to Flash sector / page

- Flash Memory Management
  - Block/Page management
  - Cache scheme

- Opt. Wear-leveling, Scrubbing

ONFi Channel

Technology-Dependent

- EZ NAND Controller
  - (ECC, Flash Device Management)

Flash Device Management:

- ECC, soft-error recovery
- Flash Operation disturbs (Read, Program) - Retries
- Off-Load Corrected Copy

(possibly later, not in EZ NAND 2.3):

- Opt. Bad Block Management
- Opt. Wear-leveling, Scrubbing

may be in the same package
ONFi / EZ NAND changes
Summary of Changes

- Support for EZ NAND features indicated in the Parameter Page
- **ECC Off-Load** – Host Controller no longer needs to support various ECC levels
- **Read Retry** – using technology dependent tricks
- **Corrected Copy** – allows LUN-LUN and plane-plane Copyback
  - preserve semantics of legacy Copyback Read and Copyback Program commands
- Status Register: Read **FAIL** and **CSP/Threshold**
  - failure and near failure status for Read commands to enable ECC offload
- Signal name standardization and “multi-plane” reference
- Parametric extensions to accommodate a **controller** (Reset timing & ICC specs)
  - For reset operations, the \texttt{tRST} value shall be adjusted to allow time for boot code load & device init
  - The **ICC current parameters** are modified to allow for additional current due to the **controller**
  - Worst case timing for Reads (allowing Retry)
- \texttt{VDDi} pin - output for bypass \texttt{CAP} for controller core supply

*No new commands, just modes or options, and independent of bus speed or async/sync*
# Parameter Page changes for EZ NAND

<table>
<thead>
<tr>
<th>Byte</th>
<th>O/M</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Revision information and features block</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 4-5  | M   | Revision number  
|      |     | 6-15 Reserved (0)  
|      |     | 5  1 = supports ONFI version 2.3  
|      |     | 0-4 same as ONFI version 2.2 |
| 6-7  | M   | Features supported  
|      |     | 10-15 Reserved (0)  
|      |     | 9  1 = supports EZ NAND function  
|      |     | 0-8 same as ONFI version 2.2 |
| 8-9  | M   | Optional commands supported  
|      |     | 10-15 Reserved (0)  
|      |     | 2-9 same as ONFI version 2.2  
|      |     | 1  1 = supports Read Cache commands (not supported by EZ NAND, shall clear to 0)  
|      |     | 0  1 = supports Page Cache Program command (not supported by EZ NAND, shall clear to 0) |
| **Memory organization block** |
| 112  | M   | Number of bits ECC correctability – EZ NAND shall clear to 0, indicating that the target returns corrected data to the host. |
| 115  | O   | EZ NAND support  
|      |     | 3-7 Reserved (0)  
|      |     | 2  1 = Requires Copyback Adjacency  
|      |     | 1  1 = supports Copyback for other planes & LUNs  
|      |     | 0  1 = supports enable/disable of automatic retries |
| 116-127 | | Reserved (0) |
| **Electrical parameters block** |
| 137-138 | M   | $t_{R}$ Maximum page read time (µs) – EZ NAND may use differently – this is $t_{R}$ Maximum at end of life, related to the UBER specified for the device. |
| 156-157 | O   | $t_{R}$ Typical page read time for EZ NAND (µs) - For devices that include multiple bits per cell in the NAND used, this value is an average of the $t_{R}$ typical values for the pages (e.g. lower and upper pages). |
| 158-163 | | Reserved (0) |
ECC Off-Load to EZ NAND Controller

**EZ NAND Page Buffer** - buffer inside EZ NAND controller that provides for temporary storage of data that is transferred between the Host and the **NAND Page Register**

**Program Example:**
- Host writes to EZ NAND Page buffer with 80h CMD, addr, data
- 10h CMD initiates data transfer to flash through ECC Encoder
- EZ NAND controller indicates success or FAIL in **LUN status register**

**Read Example:**
- Host initiates Read CMD with 00h, addr, 30h
- EZ NAND controller reads from flash, transfers data through ECC Decoder and into Page buffer
- Host polls **LUN status register** for RDY/BSY – EZ NAND controller indicates success or FAIL
- Host reads from EZ NAND Page buffer
Local Read Retry (after ECC failure)

- EZ NAND default is to perform Auto-retry on Read – may be disabled
- Host expects Read Retry at \textit{tR Maximum value} for Worst case effort - “heroics”
- Parameter Page entry for \textit{tR Typical value} for nominal “corrected” Read time
  - Host adjusts Read polling timers to \textit{tR Typical}, but allows for \textit{tR Maximum value}

<table>
<thead>
<tr>
<th>EZ NAND Control Feature Parameter 0x50</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\textbf{Retry Disable (RD):}

- If cleared to zero (default), then the EZ NAND device may automatically perform retries during error conditions at its discretion
  - If an EZ NAND controller executes an automatic retry, the \textit{Typical page read time (tR)} may be exceeded
- If set to one, then the EZ NAND device \textbf{shall not} automatically perform retries
  - If automatic retries are disabled, the device may exceed the UBER specified
  - Automatic retries shall only be disabled if the device supports this capability as indicated in the parameter page
Data Copy/Move by EZ NAND Controller

Flash Memory Management (by Host) typically performs:

**Many NAND Copy Operations**

EZ NAND Controller can provide **Off-Load data copy** to service/ accelerate the Host’s Flash Memory Management function

- Reduces data movement over Host Controller ONFI channel (bus 0)
- can off-load Host Controller involvement in frequent Flash copy operations

  - Copyback Local and Regenerate ECC to prevent error propagation
  - Copyback Local with Data modification (and Generate New ECC)

8/19/10
Host Off-Load (to controller) Copy Operations

- **Copyback command Functional Extensions to ONFi v2.2** - via *bus1* transfer
  - Within plane (same LUN) – same as v2.2, but ECC correction **in EZ NAND controller**
  - Plane-to-plane (same LUN), with ECC correction – **new feature in v2.3**
  - LUN-to-LUN (different LUN, same/different plane), with ECC correction – **new feature in v2.3**

- **Copyback commands** – with no Host (*bus0*) transfer
  - Performance optimization

- **Retains Copyback Program with data modification**
  - Host may modify EZ NAND Page Buffer during Copyback Program
### ONFi Status Register changes

<table>
<thead>
<tr>
<th>Value</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status Register</td>
<td>WP_n</td>
<td>RDY</td>
<td>ARDY</td>
<td>VSP</td>
<td>CSP</td>
<td>R</td>
<td>FAILC</td>
<td>FAIL</td>
</tr>
</tbody>
</table>

- **FAIL**: If set to one, then the last command failed. If cleared to zero, then the last command was successful. For raw NAND operation, bit is only valid for program and erase operations. For EZ NAND operation, bit is valid for read, program, and erase operations.

- **FAILC**: For EZ NAND operation, this bit is not used (cache commands are not supported with EZ NAND).

- **CSP**: Command Specific: This bit has command specific meaning.

  For EZ NAND read operations, if CSP (Threshold) bit is set to one then the last read operation exceeded the ECC threshold and the host should take appropriate action (e.g. rewrite the data to a new location). When FAIL is set to one, the CSP (Threshold) bit is don’t care.

  For all other operations, this bit is reserved.

- **ARDY**: For EZ NAND operation, this bit is not used (cache commands are not supported with EZ NAND).
Spec parameter changes
Power-On Requirements

Once $V_{CC}$ and $V_{ccQ}$ reach the $V_{CC}$ minimum and $V_{ccQ}$ minimum values, respectively, listed in Table and power is stable, the R/B_n signal shall be valid after $RB\_valid\_Vcc$ and shall be set to one (Ready) within $RB\_device\_ready$, as listed in Table 2.

R/B_n is undefined until 50 µs has elapsed after $V_{CC}$ has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Raw NAND</th>
<th>EZ NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>$RB_valid_Vcc$</td>
<td>10 µs</td>
<td>250 µs</td>
</tr>
<tr>
<td>$RB_device_ready$</td>
<td>1 ms</td>
<td>2 ms</td>
</tr>
</tbody>
</table>

\[V_{cc} = V_{cc\_min}\]
\[\geq 0 \mu s \text{ (min)}\]
\[\text{Vcc ramp starts}\]
\[\text{Reset (FFh) is issued}\]
(tRST) Timing Parameters per Modes 0-5

### Asynchronous Timing Modes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mode 0</th>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Mode 3</th>
<th>Mode 4 (EDO)</th>
<th>Mode 5 (EDO)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>100</td>
<td>50</td>
<td>35</td>
<td>30</td>
<td>25</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>~10</td>
<td>~20</td>
<td>~28</td>
<td>~33</td>
<td>~40</td>
<td>~50</td>
<td>MHz</td>
</tr>
<tr>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td></td>
</tr>
<tr>
<td>tRST (raw NAND)</td>
<td>—</td>
<td>5000</td>
<td>—</td>
<td>5/10/ 500</td>
<td>—</td>
<td>5/10/ 500</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>µs</td>
</tr>
<tr>
<td>tRST^2 (EZ NAND)</td>
<td>—</td>
<td>250000</td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>µs</td>
</tr>
</tbody>
</table>

**NOTE 2:** If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using LUN Reset (FAh) then the values are as shown.

### Source synchronous Timing Modes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Mode 0</th>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Mode 3</th>
<th>Mode 4</th>
<th>Mode 5</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>50</td>
<td>30</td>
<td>20</td>
<td>15</td>
<td>12</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>~20</td>
<td>~33</td>
<td>~50</td>
<td>~66</td>
<td>~83</td>
<td>~100</td>
<td>MHz</td>
</tr>
<tr>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td>Min Max</td>
<td></td>
</tr>
<tr>
<td>tRST (raw NAND)</td>
<td>—</td>
<td>5/10/ 500</td>
<td>—</td>
<td>5/10/ 500</td>
<td>—</td>
<td>5/10/ 500</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>µs</td>
</tr>
<tr>
<td>tRST^2 (EZ NAND)</td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>—</td>
<td>150/ 500</td>
<td>µs</td>
</tr>
</tbody>
</table>

**NOTE 2:** If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Synchronous Reset (FCh) or LUN Reset (FAh) then the values are as shown.
## EZ NAND: DC and Operating Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array read current</td>
<td>ICC1</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>85</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ1</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>Array program current</td>
<td>ICC2</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>85</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ2</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>Array erase current</td>
<td>ICC3</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>85</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ3</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>I/O burst read current</td>
<td>ICC4(^R)</td>
<td>LUN</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ4(^R)</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>I/O burst write current</td>
<td>ICC4(^W)</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>45</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ4(^W)</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>Bus idle current</td>
<td>ICC5</td>
<td>Per LUN</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ICCQ5</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Standby current, CMOS</td>
<td>ISB</td>
<td>CE(_n)=VccQ-0.2V, CE(_p)=VccQ-0.2V, WP(_n)=0V/VccQ</td>
<td>Per LUN</td>
<td>-</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>ISBQ</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>1000</td>
<td>µA</td>
</tr>
<tr>
<td>Staggered power-up current</td>
<td>IST(^1)</td>
<td>CE(_n)=VccQ-0.2V, tRise = 1 ms, cLine = 0.1 µF</td>
<td>Per LUN</td>
<td>-</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ISTQ</td>
<td>Controller</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Refer to Appendix C for an exception to the IST current requirement.
2. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to Appendix D.
3. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + ICC4\(^R\) on Vcc and ICCQ1 on VccQ; for a cached write this value is ICC2(active) + ICC4\(^W\) on Vcc and ICCQ2 on VccQ.
4. For ICC4\(^R\) the test conditions in Appendix D. specify IOUT = 0 mA and requires static outputs with no output switching. When outputs are not static, additional VccQ current will be drawn that is highly dependent on system configuration. IccQ may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C\(_L\) * VccQ * frequency), where C\(_L\) is the capacitive load.

8/19/10
Summary

- **EZ NAND – The Key Feature of ONFi 2.3**
  - Offers optimal partition / flexibility
    - FMM – remains in Host – Optimized per application
    - FDM, ECC – handled by EZ NAND Module
  - Technology-Dependent boundary
    - “hides” complexity of NAND from Host – ECC scheme, etc.
  - Optimized per NAND type (Lithography, Vendor, Bits/cell)

- **Minimal changes to support**
  - Leverage ONFi raw NAND infrastructure – no new commands!
  - New capabilities of EZ NAND Module:
    - ECC Off-Load; Read Retry; Off-Load Corrected Copy, Flexible Copy (plane/LUN)
  - Parameter Page, Status Register
  - Parametric extensions for added controller, boot-up
Achievable, Beneficial

Flexible Host Controller

(optimized Memory Management & Host Application)

ONFi = Host to Flash I/F

ECC & FDM

Host I/F:

(SATA, SAS, PCIe, XYZ...)

Flash Vendor A

5x nm

SLC

MLC

8LC

3x nm

SLC

MLC

8LC

2x nm

SLC

MLC

8LC

Flash Vendor B

5x nm

SLC

MLC

8LC

3x nm

MLC

8LC

2x nm

MLC

8LC

Flash Vendor C

5x nm

SLC

MLC

8LC

3x nm

SLC

MLC

8LC

2x nm

SLC

MLC

8LC

Flash Vendor D

5x nm

SLC

MLC

8LC

3x nm

SLC

MLC

8LC

2x nm

SLC

MLC

8LC

8/19/10
Thank you!

Please visit [www.onfi.org](http://www.onfi.org) for more information on ONFi v2.3 and EZ NAND