



The New EZ NAND in ONFi v2.3

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Systems Architecture

SanDisk

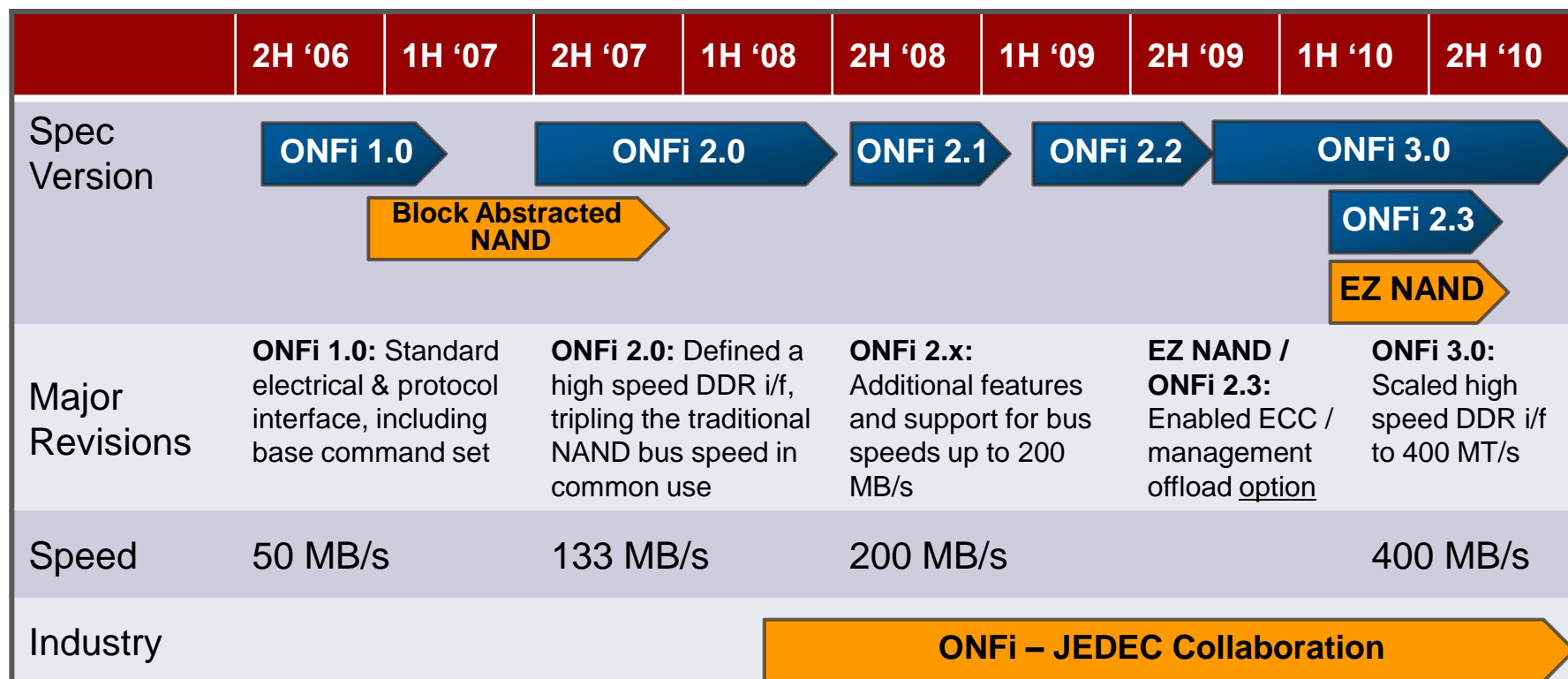
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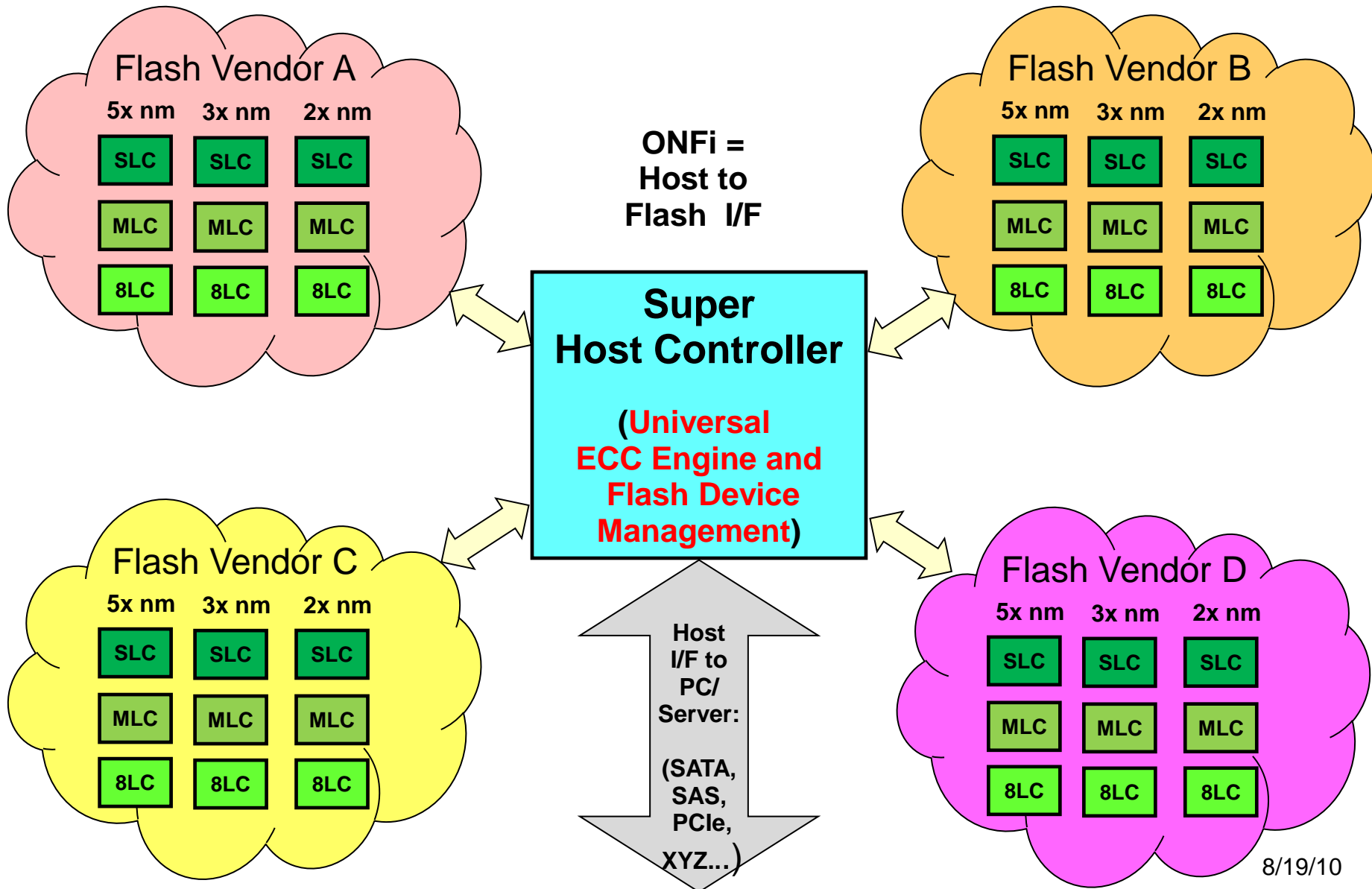
- ONFi Overview
- Ultimate Challenge...
- What is EZ NAND?
 - Flash Memory Management vs. Device Management
 - Raw NAND vs. BA vs. EZ NAND
 - Technology-Dependent boundary
- ONFi 2.3 / EZ NAND - Minimal Changes

ONFi Workgroup Overview & Results

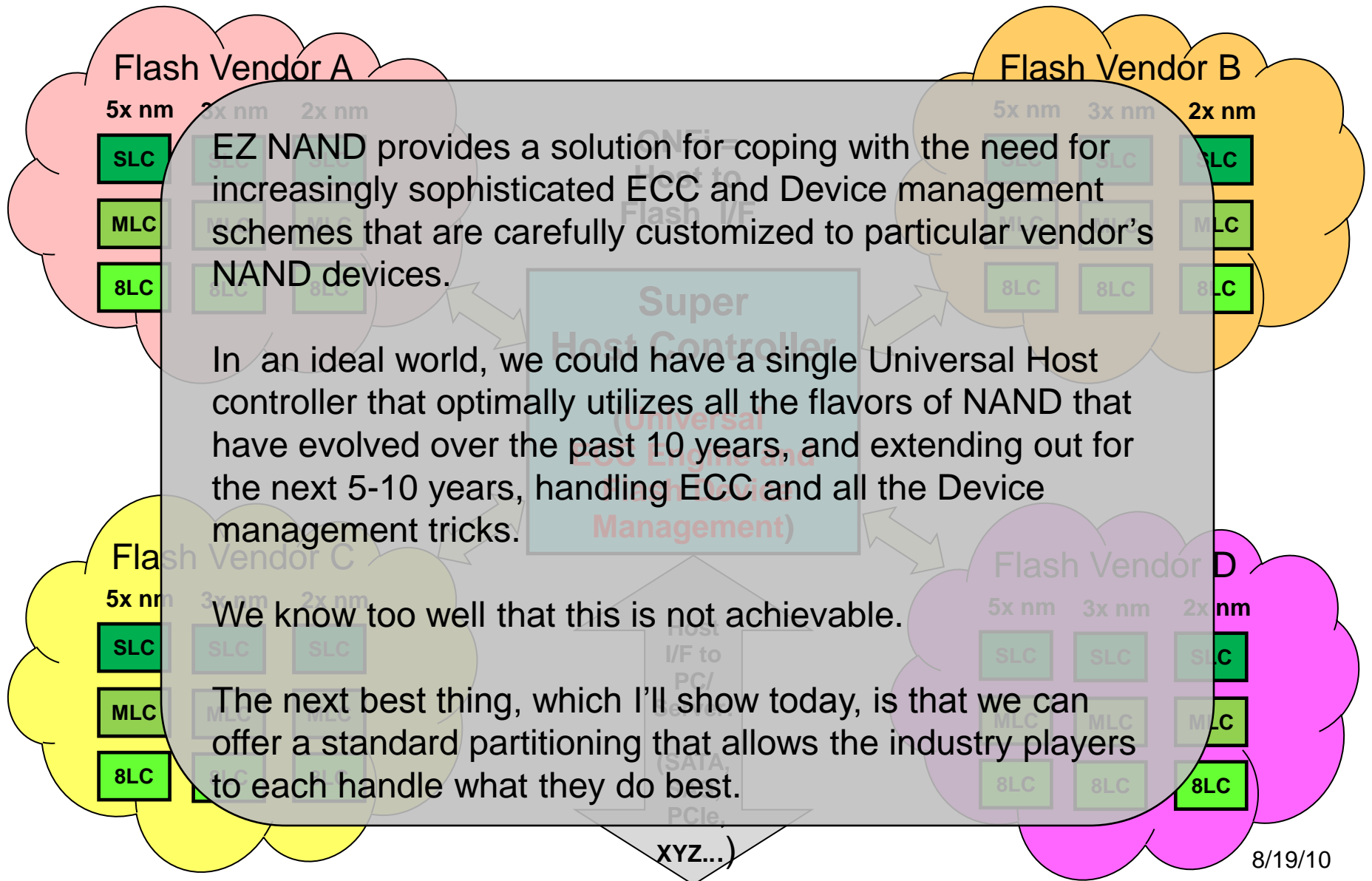
- ONFi continues to deliver **innovation & interoperability** enabling faster NAND adoption and **increasing performance**



Ultimate Challenge – The Super Controller



Ultimate Challenge – The Super Controller



Version 2.3 (planned release) Aug. 2010 – Main feature: **EZ NAND** function

- Areas of change:
 - Parameter Page: feature registers
 - ECC Off-Load
 - Read Retry
 - Corrected Copy
 - Status Register
 - Signal name standardization and “multi-plane” reference
 - Parametric extensions

* Backwards compatible to ONFi v2.2

EZ (ECC Zero) **NAND** – a NAND device / module that requires no ECC correction by the Host (ECC is handled internally to NAND package)

And EZ NAND is **Easy** to implement and support!

- Goal of EZ NAND is to create a **packaged NAND** that “hides” the **technology dependent** portions of NAND management.
- Simple ASIC stacked within a NAND package performs **NAND device management** functionality that is **lithography specific** (such as ECC and error correction), while retaining raw NAND protocol infrastructure.
- EZ NAND delivers an ECC offloaded solution with minimal command and/or protocol changes. The device **parameter page** specifies if EZ NAND is supported.

■ Technology Independent components

- **Flash Translation Layer (FTL)** – mapping from Host bus (SATA, PCI, etc.) to Flash blocks, planes, pages
- **Flash Memory Management (FMM)** - caching, garbage collection, storage optimization

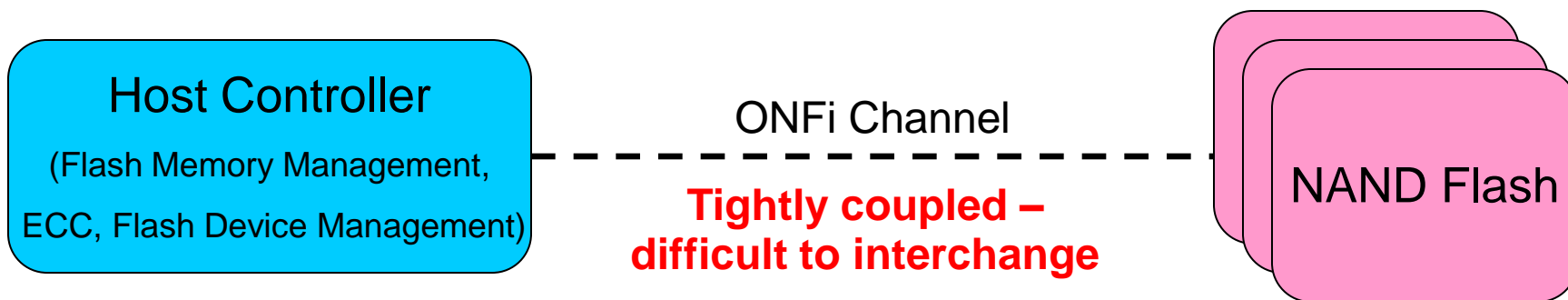
■ Technology Dependent components

- **Flash Device Management (FDM)**
 - Examples:
 - ECC, Soft-error recovery, Wear Leveling, Scrubbing
 - Variations between:
 - **Generations** (lithography – 5x, 3x, 2x, ... nm)
 - **Vendors**
 - **Bits/cell** – SLC, MLC, 3+ bits/cell
- EZ NAND parts may be offered with:
 - Different performance / endurance / quality specs

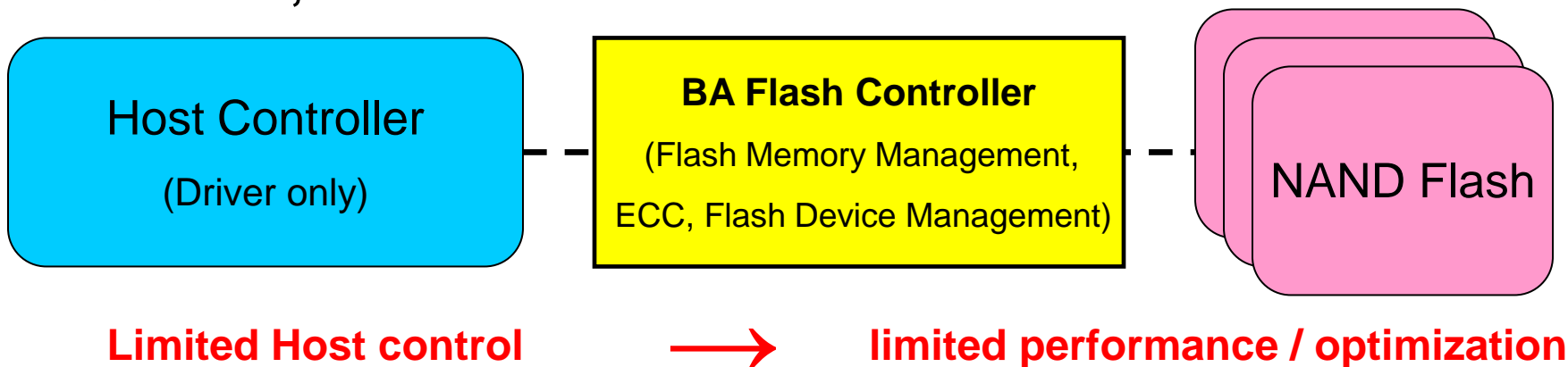
➔ **Technology Dependent issues becoming more significant and varied**

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1. **Standard ONFI / Raw NAND** – stand-alone Host Controller – Host performs all Flash control functions



2. **BA (Block Abstraction)** – BA Flash controller frees Host from **FMM** and **FDM, but ...**



3. **EZ NAND** – Host retains Memory Management function, EZ NAND controller handles Technology-Dependent Flash Device Management.

Goal: Separate **Technology Independent** and **Technology Dependent**



Optimized per Application!

Optimized per NAND type!

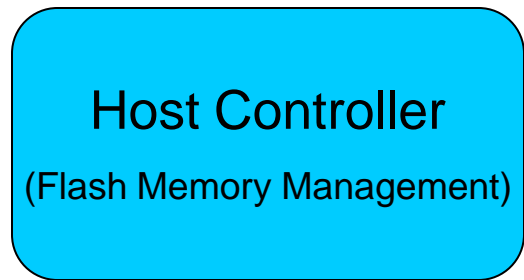
Benefits:

- Host Controller works with **multiple types**, generations (and various performance points) of Flash
- Memory Management remains in Host for best optimization **per application**

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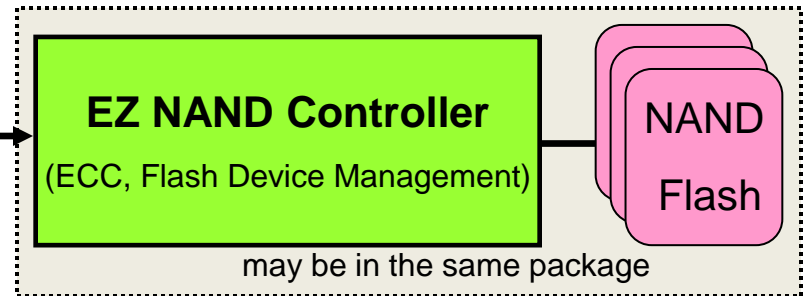
EZ NAND Module – Technology-Dependent Operations Off-Load

Technology-Independent



ONFi Channel

Technology-Dependent



- Flash Translation Layer
 - Mapping Host LBA to Flash sector / page
- **Flash Memory Management**
 - Block/Page management
 - Cache scheme
- Opt. Wear-leveling, Scrubbing

Flash Device Management:

- **ECC, soft-error recovery**
- **Flash Operation disturbs (Read, Program) - Retries**
- **Off-Load Corrected Copy**

(possibly later, not in EZ NAND 2.3):

- **Opt. Bad Block Management**
- **Opt. Wear-leveling, Scrubbing**

ONFi / EZ NAND changes

- Support for EZ NAND features indicated in the Parameter Page
- **ECC Off-Load** – Host Controller no longer needs to support various ECC levels
- **Read Retry** – using technology dependent tricks
- **Corrected Copy** – allows LUN-LUN and plane-plane Copyback
 - preserve semantics of legacy Copyback Read and Copyback Program commands
- Status Register: Read **FAIL** and **CSP/Threshold**
 - failure and near failure status for Read commands to enable ECC offload
- Signal name standardization and “multi-plane” reference
- Parametric extensions to accommodate a **controller** (Reset timing & ICC specs)
 - For reset operations, the **tRST** value shall be adjusted to allow time for boot code load & device init
 - The **ICC current parameters** are modified to allow for additional current due to the **controller**
 - Worst case timing for Reads (allowing Retry)
- VDDi pin - output for bypass CAP for controller core supply

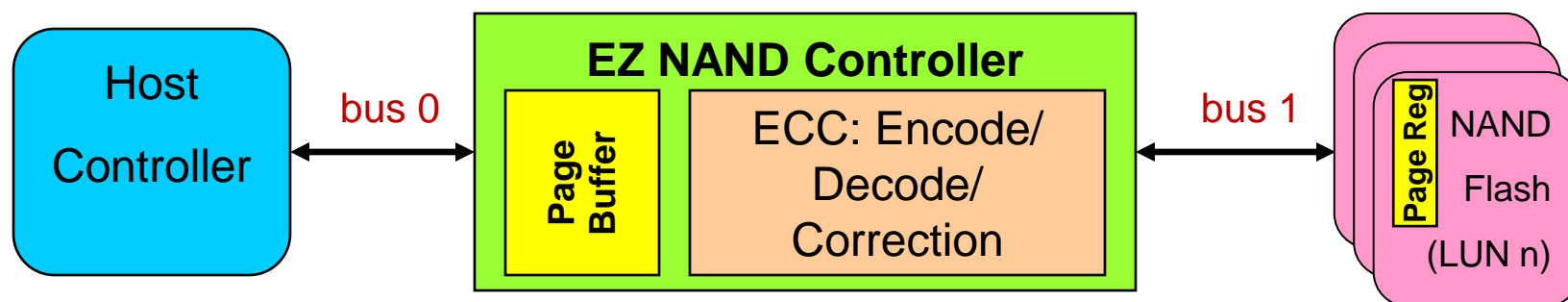
No new commands, just modes or options, and independent of bus speed or async/sync

Parameter Page changes for EZ NAND



Byte	O/M	Description
Revision information and features block		
4-5	M	Revision number 6-15 Reserved (0) 5 1 = supports ONFI version 2.3 0-4 same as ONFI version 2.2
6-7	M	Features supported 10-15 Reserved (0) 9 1 = supports EZ NAND function 0-8 same as ONFI version 2.2
8-9	M	Optional commands supported 10-15 Reserved (0) 2-9 same as ONFI version 2.2 1 1 = supports Read Cache commands (not supported by EZ NAND, shall clear to 0) 0 1 = supports Page Cache Program command (not supported by EZ NAND, shall clear to 0)
Memory organization block		
112	M	Number of bits ECC correctability – EZ NAND shall clear to 0, indicating that the target returns corrected data to the host.
115	O	EZ NAND support 3-7 Reserved (0) 2 1 = Requires Copyback Adjacency 1 1 = supports Copyback for other planes & LUNs 0 1 = supports enable/disable of automatic retries
116-127		Reserved (0)
Electrical parameters block		
137-138	M	t_R Maximum page read time (μs) – EZ NAND may use differently – this is t_R Maximum at end of life, related to the UBER specified for the device.
156-157	O	t_R Typical page read time for EZ NAND (μs) - For devices that include multiple bits per cell in the NAND used, this value is an average of the t_R typical values for the pages (e.g. lower and upper pages).
158-163		Reserved (0)

ECC Off-Load to EZ NAND Controller



EZ NAND Page Buffer - buffer inside EZ NAND controller that provides for temporary storage of data that is transferred between the Host and the **NAND Page Register**

Program Example:

- Host writes to EZ NAND Page buffer with 80h CMD, addr, data
- 10h CMD initiates data transfer to flash through ECC Encoder
- EZ NAND controller indicates success or FAIL in **LUN status register**

Read Example:

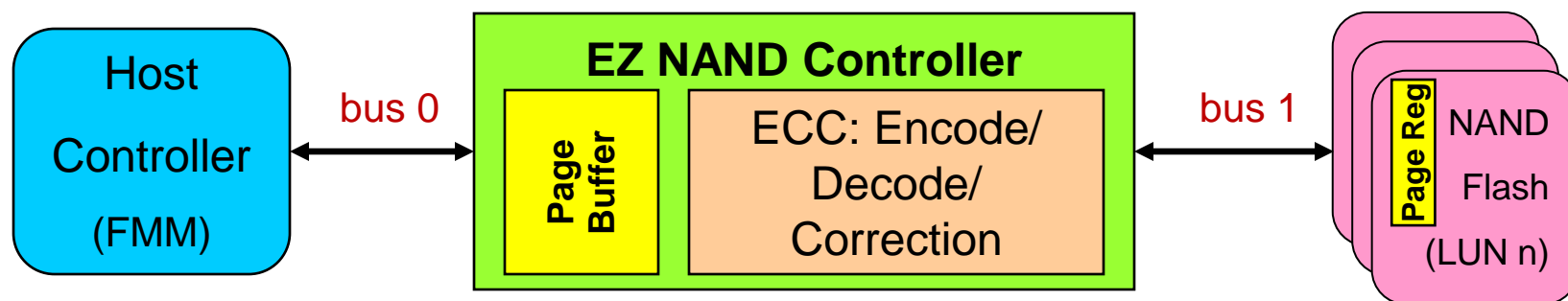
- Host initiates Read CMD with 00h, addr, 30h
- EZ NAND controller reads from flash, transfers data through ECC Decoder and into Page buffer
- Host polls **LUN status register** for RDY/BSY – EZ NAND controller indicates success or FAIL
- Host reads from EZ NAND Page buffer

- EZ NAND default is to perform Auto-retry on Read – may be disabled
- Host expects Read Retry at “**tR Maximum value**” for Worst case effort - “heroics”
- Parameter Page entry for “**tR Typical value**” for nominal “corrected” Read time
 - Host adjusts Read polling timers to **tR Typical**, but allows for **tR Maximum value**

EZ NAND Control Feature Parameter 0x50	7	6	5	4	3	2	1	0
P1	Reserved (0)							RD

Retry Disable (RD):

- If cleared to zero (default), then the EZ NAND device may automatically perform retries during error conditions at its discretion
 - If an EZ NAND controller executes an automatic retry, the **Typical page read time (tR)** may be exceeded
- If set to one, then the EZ NAND device **shall not** automatically perform retries
 - If automatic retries are disabled, the device may exceed the UBER specified
 - Automatic retries shall only be disabled if the device supports this capability as indicated in the parameter page

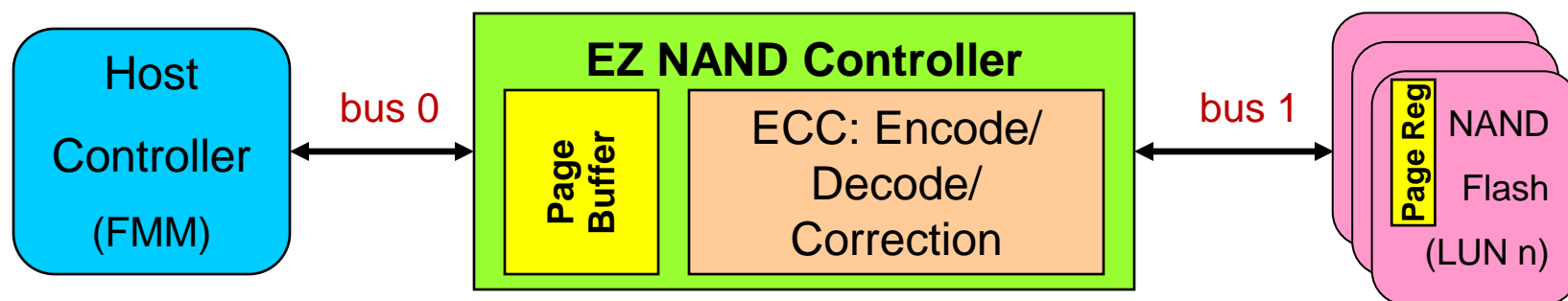


Flash Memory Management (by Host) typically performs:

Many NAND Copy Operations

EZNAND Controller can provide **Off-Load data copy** to service/ accelerate the Host's Flash Memory Management function

- ➔ Reduces data movement over Host Controller ONFI channel (**bus 0**)
- ➔ can off-load Host Controller involvement in frequent Flash copy operations
 - **Copyback Local** and Regenerate ECC to prevent error propagation
 - **Copyback Local** with Data modification (and Generate New ECC)



Host Off-Load (to controller) Copy Operations

- **Copyback command Functional Extensions to ONFi v2.2 - via bus1 transfer**
 - Within plane (same LUN) – same as v2.2, but ECC correction **in EZ NAND controller**
 - Plane-to-plane (same LUN), with ECC correction – **new feature in v2.3**
 - LUN-to-LUN (different LUN, same/different plane), with ECC correction – **new feature in v2.3**
- **Copyback commands – with no Host (bus0) transfer**
 - Performance optimization
- **Retains Copyback Program with data modification**
 - Host may modify EZ NAND Page Buffer during Copyback Program

ONFi Status Register changes

Value	7	6	5	4	3	2	1	0
Status Register	WP_n	RDY	ARDY	VSP	CSP	R	FAILC	FAIL

- FAIL** If set to one, then the last command failed. If cleared to zero, then the last command was successful. For raw NAND operation, bit is only valid for program and erase operations. For EZ NAND operation, bit is valid for read, program, and erase operations.
- FAILC** For EZ NAND operation, this bit is not used (cache commands are not supported with EZ NAND).
- CSP** Command Specific: This bit has command specific meaning.
- For EZ NAND read operations, if CSP (Threshold) bit is set to one then the last read operation exceeded the ECC threshold and the host should take appropriate action (e.g. rewrite the data to a new location). When FAIL is set to one, the CSP (Threshold) bit is don't care.
- For all other operations, this bit is reserved.
- ARDY** For EZ NAND operation, this bit is not used (cache commands are not supported with EZ NAND).

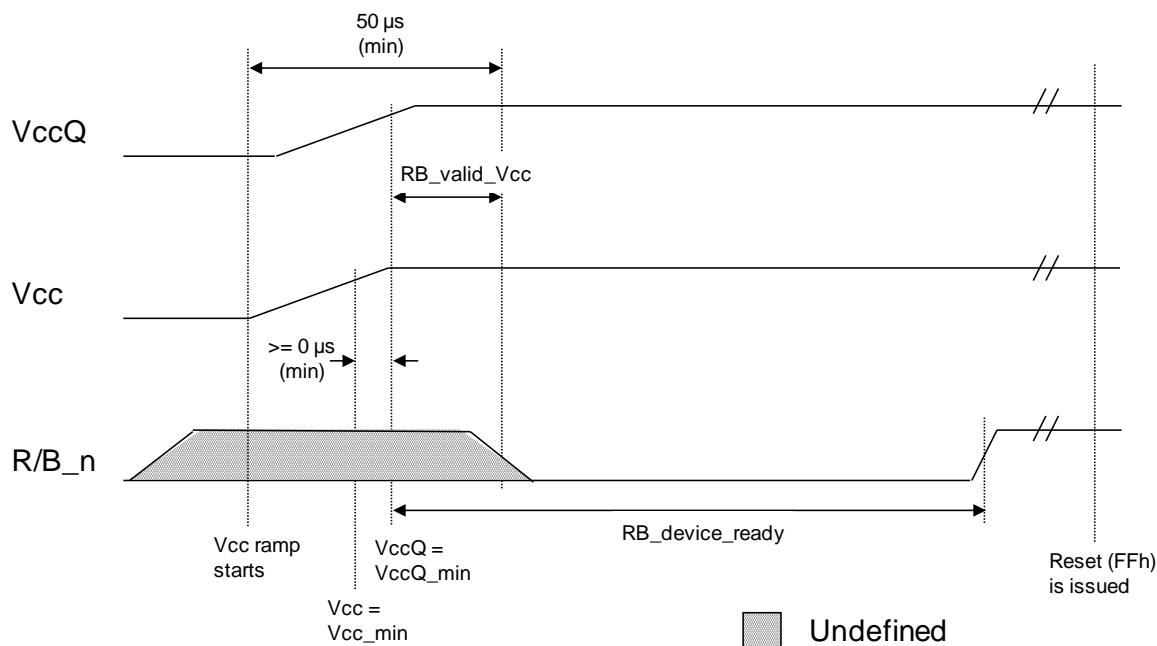
Spec parameter changes

Power-On Requirements

Once V_{CC} and V_{CCQ} reach the V_{CC} minimum and V_{CCQ} minimum values, respectively, listed in Table and power is stable, the R/B_n signal shall be valid after **RB_valid_Vcc** and shall be set to one (Ready) within **RB_device_ready**, as listed in Table 2.

R/B_n is undefined until 50 μ s has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Parameter	Raw NAND	EZ NAND
RB_valid_Vcc	10 μ s	250 μ s
RB_device_ready	1 ms	2 ms



(tRST) Timing Parameters per Modes 0-5



Asynchronous Timing Modes

Parameter	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4 (EDO)		Mode 5 (EDO)		Unit
	100		50		35		30		25		20		ns
	~10		~20		~28		~33		~40		~50		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tRST (raw NAND)	—	5000	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	μs
tRST ² (EZ NAND)	—	250000	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	μs

NOTE 2: If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using LUN Reset (FAh) then the values are as shown.

Source synchronous Timing Modes

Parameter	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
	50		30		20		15		12		10		ns
	~20		~33		~50		~66		~83		~100		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tRST (raw NAND)	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	—	5/10/ 500	μs
tRST ² (EZ NAND)	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	—	150/ 150/ 500	μs

NOTE 2: If the reset is invoked using a Reset (FFh) command then the EZ NAND device has 250 ms to complete the reset operation regardless of the timing mode. If the reset is invoked using Synchronous Reset (FCh) or LUN Reset (FAh) then the values are as shown.

EZ NAND: DC and Operating Characteristics



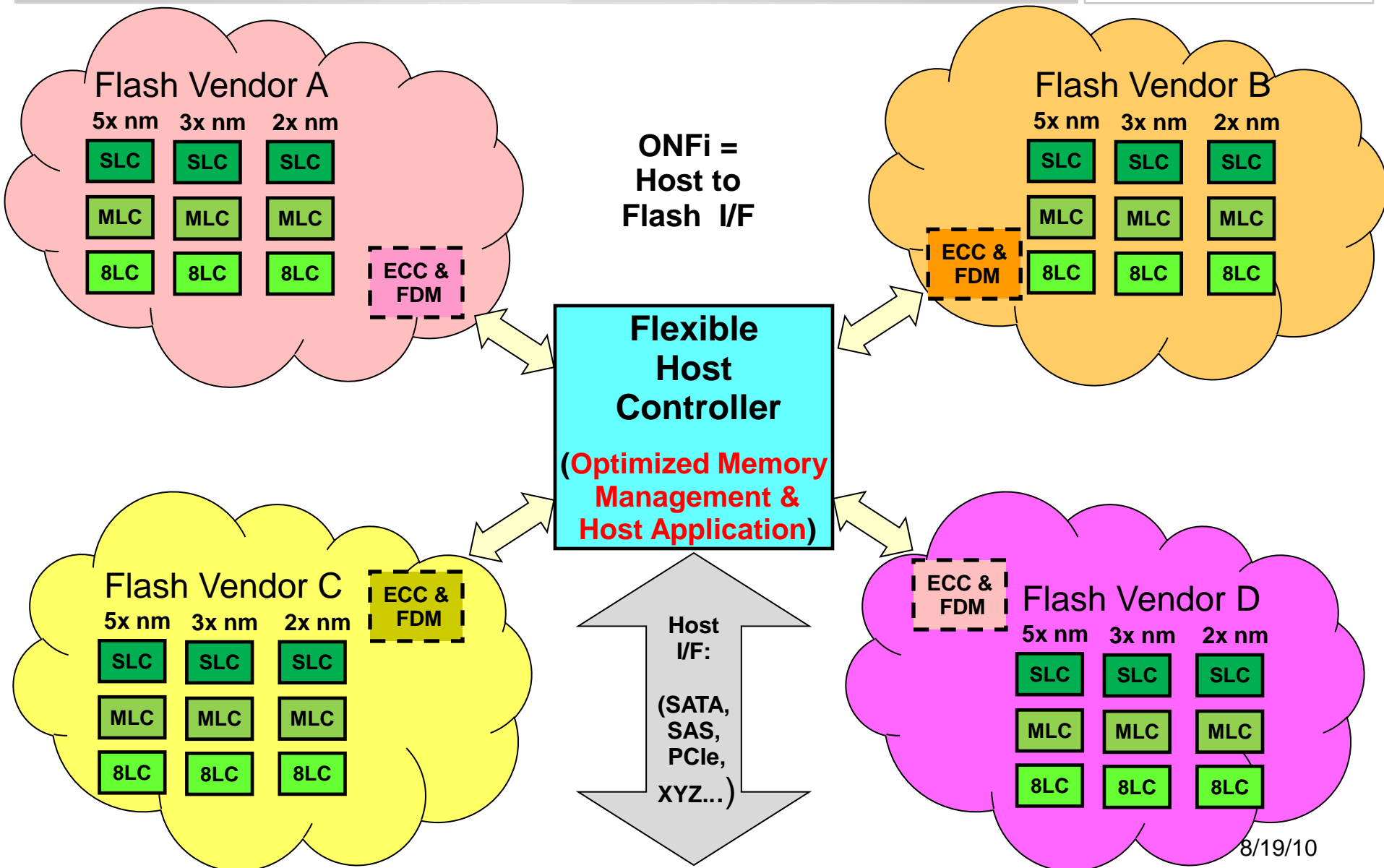
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Array read current	ICC1	Refer to Appendix D	Per LUN	-	-	85	mA
	ICCQ1		Controller	-	-	200	
	ICCQ1		Per LUN	-	-	15	
Array program current	ICC2		Per LUN	-	-	85	mA
	ICCQ2		Controller	-	-	75	
	ICCQ2		Per LUN	-	-	15	
Array erase current	ICC3		Per LUN	-	-	85	mA
	ICCQ3		Controller	-	-	75	
	ICCQ3		Per LUN	-	-	15	
I/O burst read current	ICC4 _R ⁴		LUN	-	-	50	mA
	ICCQ4 _R ⁴		Controller	-	-	50	
I/O burst write current	ICC4 _W		LUN	-	-	50	mA
	ICCQ4 _W		Controller	-	-	50	
Bus idle current	ICC5		Per LUN	-	-	45	mA
	ICCQ5		Controller	-	-	10	
	ICCQ5	Per LUN	-	-	15		
Standby current, CMOS	ISB	CE _n =VccQ-0.2V, WP _n =0V/VccQ	Per LUN	-	-	50	µA
	ISBQ		Controller	-	-	1000	
Staggered power-up current	IST ¹	CE _n =VccQ-0.2V tRise = 1 ms cLine = 0.1 µF	Per LUN	-	-	10	mA
	ISTQ		Controller	-	-	20	

NOTE:

1. Refer to **Appendix C** for an exception to the IST current requirement.
2. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to **Appendix D**
3. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + ICC4_R on Vcc and ICCQ1 on VccQ; for a cached write this value is ICC2(active) + ICC4_W on Vcc, and ICCQ2 on VccQ.
4. For ICC4_R the test conditions in **Appendix D**. specify IO_{UT} = 0 mA and requires static outputs with no output switching. When outputs are not static, additional VccQ current will be drawn that is highly dependent on system configuration. IccQ may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C_L * VccQ * frequency), where C_L is the capacitive load.

- **EZ NAND – The Key Feature of ONFi 2.3**
 - Offers optimal partition / flexibility
 - FMM – remains in Host – Optimized per application
 - FDM, ECC – handled by EZ NAND Module
 - Technology-Dependent boundary
 - “hides” complexity of NAND from Host – ECC scheme, etc.
 - Optimized per NAND type (Lithography, Vendor, Bits/cell)

- **Minimal changes to support**
 - Leverage ONFi raw NAND infrastructure – no new commands!
 - New capabilities of EZ NAND Module:
 - ECC Off-Load; Read Retry; Off-Load Corrected Copy, Flexible Copy (plane/LUN)
 - Parameter Page, Status Register
 - Parametric extensions for added controller, boot-up



Thank you!

Please visit www.onfi.org for more information on
ONFi v2.3 and EZ NAND

