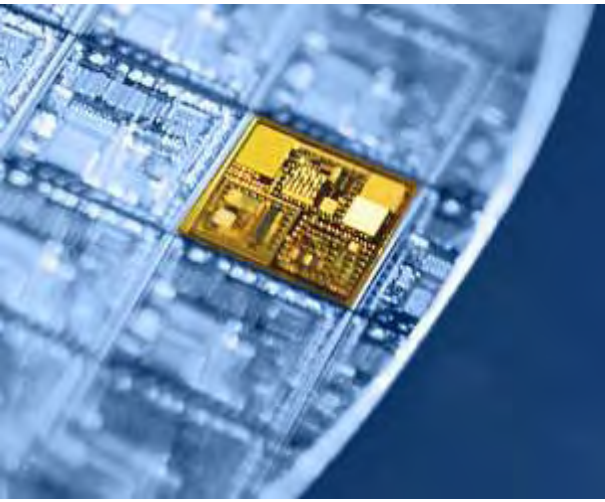


CMOS NVM Extended Reliability Performance

Flash Memory Summit

August 2010

THE SEMICONDUCTOR INDUSTRY'S TRUSTED IP PARTNER

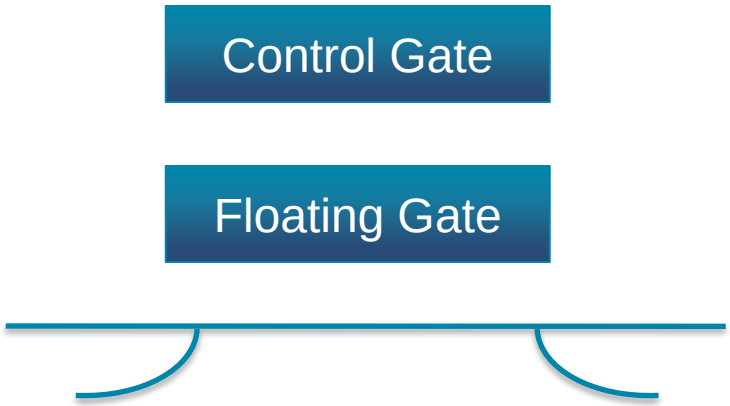
Outline

- Introduction – What is CMOS NVM?
- How do we guarantee Manufacturability?
- Extended reliability results
- Conclusions

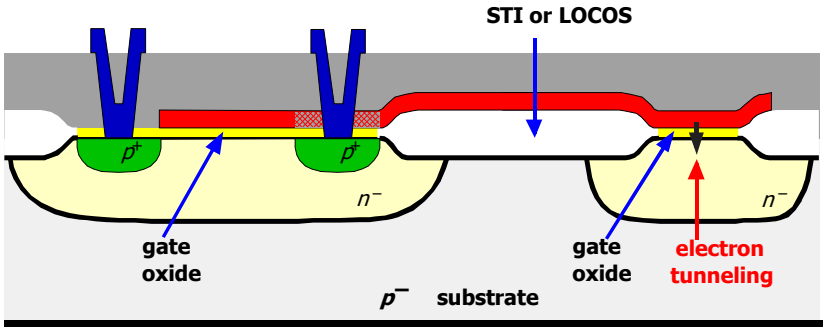
Introduction : What is CMOS NVM?

- **CMOS NVM**: Embedded NVM that is built in a standard logic CMOS process (single poly) with no additional masks / processing steps

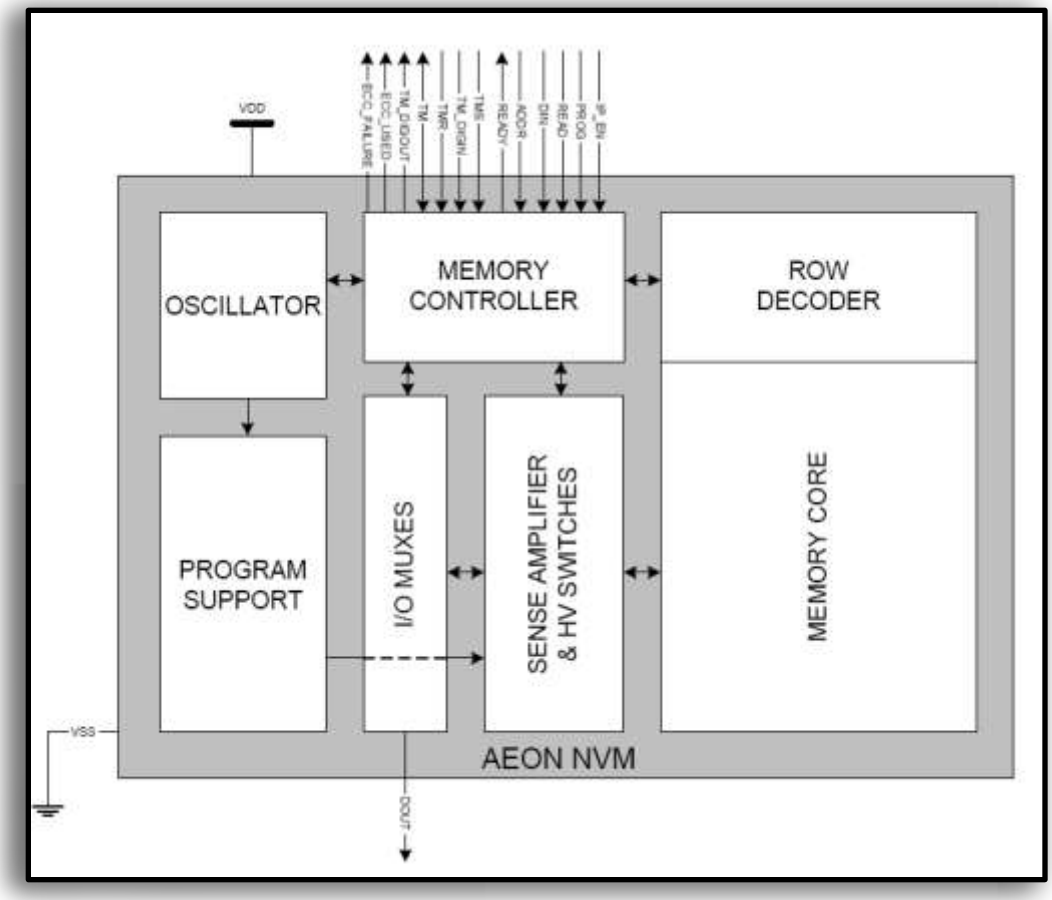
Flash / EEPROM



LNVM



Introduction : AEON® Product Families



- Fully contained IP
- NVM array
- Analog blocks
  - Charge pump
  - Bias/oscillator
  - HV switch
  - Sense Amplifier
- Digital controller
- Test Modes

Manufacturability Validation

- Is the IP manufacturable?
- Parametric performance across process splits
- Margin to specification?
- Update specification if needed

- Does the IP meet qualification standards?
- Automotive vs. consumer
- Multiple lots tested
- Gage of quality

- Does the IP meet Reliability target?
- Understanding of failure mode
- Reliability models

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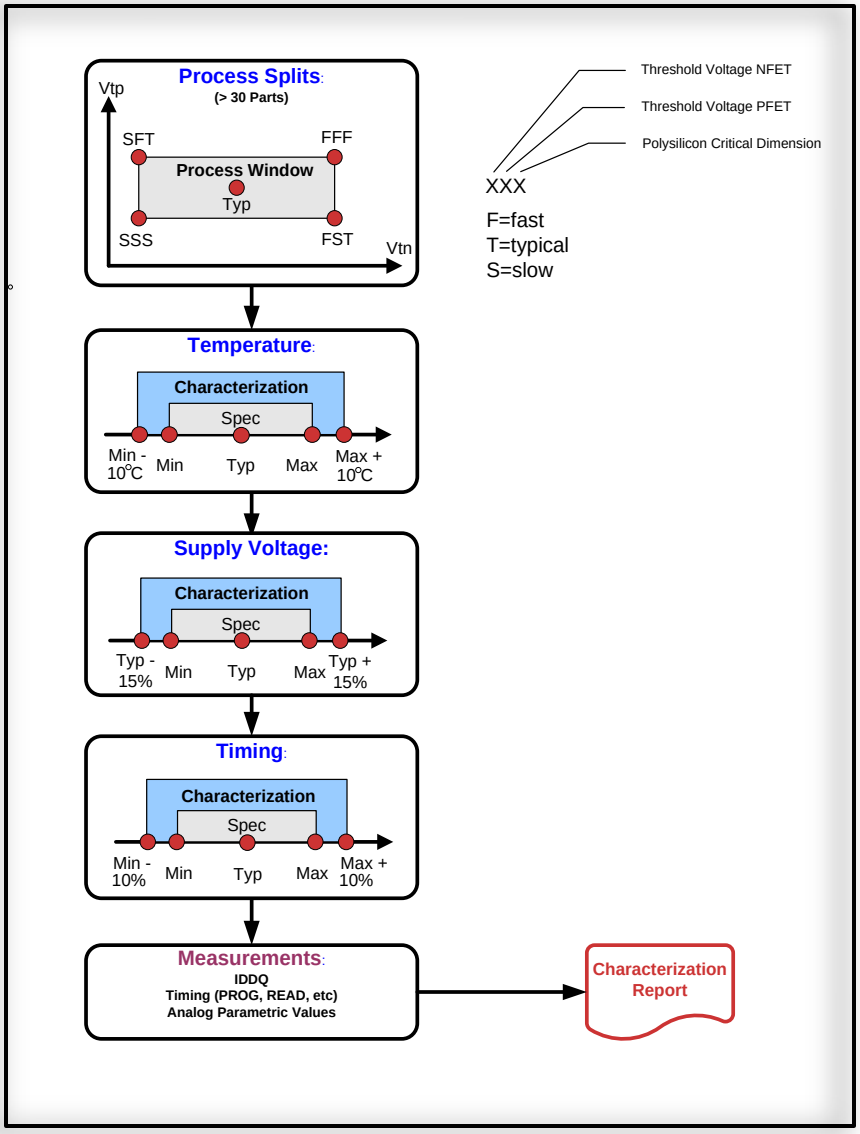
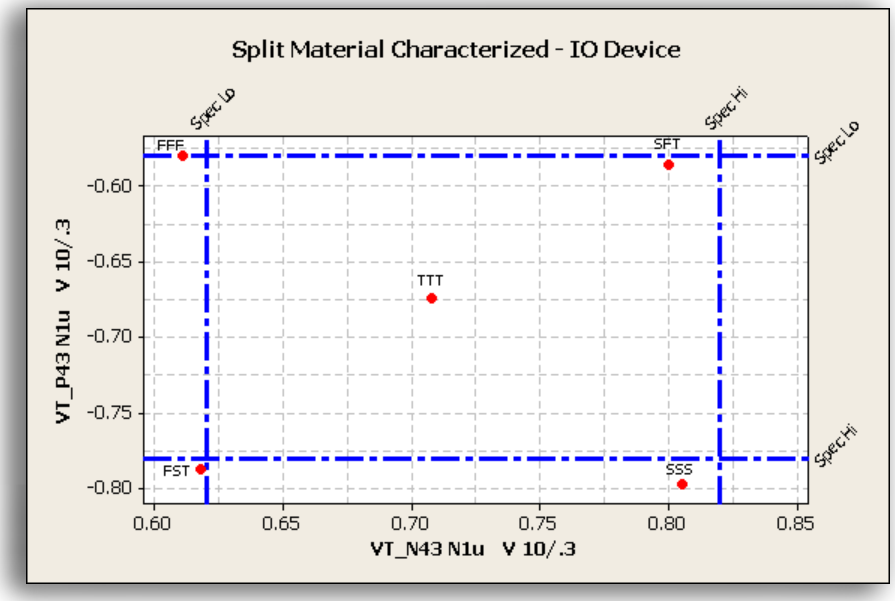
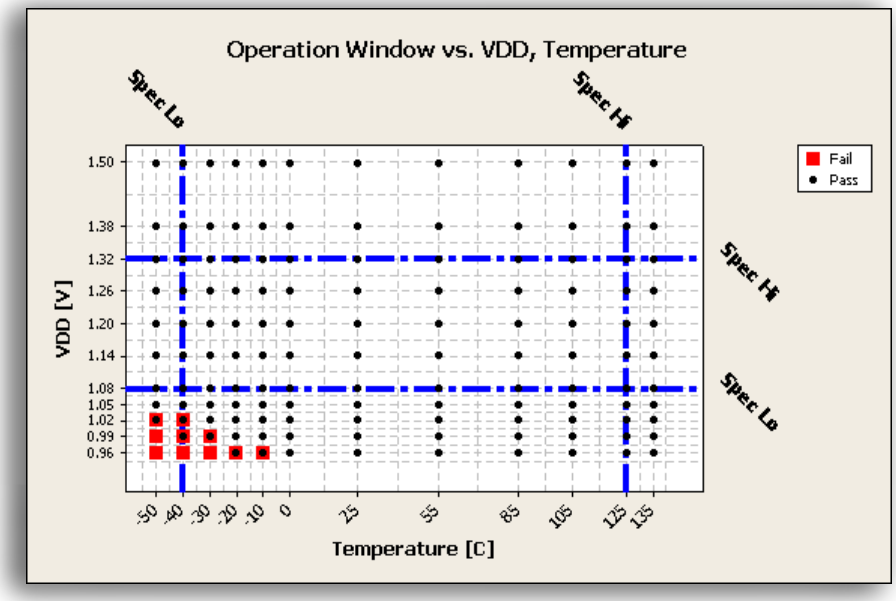
Characterization



- Process skew wafers
  - Vt and poly CD splits
  - Oxide splits
- Beyond spec temperature
- Beyond spec voltage
- Key parameters tested
  - Yield
  - Program / Read times
  - Current consumption
  - Internal Analog blocks
  - Retention
  - Endurance
  - Disturb

Characterization Example : Functionality Shmoo





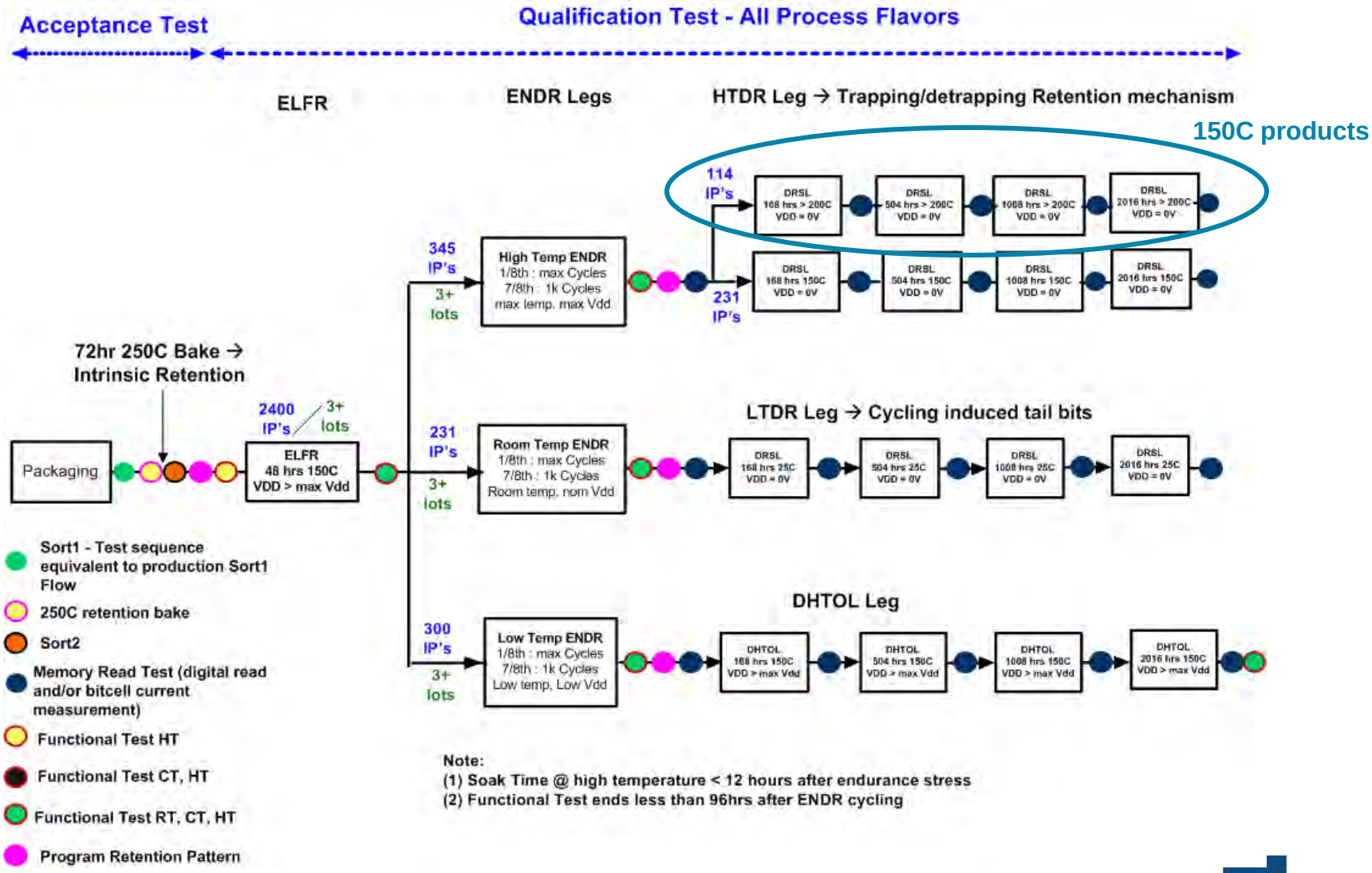
- Shmoo plot validates IP functionality (Prog/Read) on all process split above and beyond operating window
- Highlight manufacturing margin and IP sensitivity to process/operating conditions
- Production test flow limits based on characterization results

Qualification – Many Standards

	ENDR CT	ENDR RT	ENDR HT	HTOL	Retention HT	Retention LT
AEC Q100 G AEC Q100-005 C	3 x 77 Worst Case Condition			3 x 77	3 x 77	
JESD47F		3 x 38	3 x 39	3 x 77	3 x 39	3 x 38
TSMC 9000			3 x 77	3 x 100	3 x 77	
Virage Logic	3 x 100	3 x 77	3 x 77	3 x 100	3 x 77 + 3 x 38	3 x 77

- VIRL qualification approach is a superset of key standards with respect to NVM testing
  - Automotive : AEC Q100 RevG
  - Consumer / Industrial : JEDEC JESD47G
  - Foundry : e.g. TSMC IP9000

Automotive Qualification Plan (EEPROM)



Is passing qual sufficient to guarantee quality/reliability targets for the NVM IP?

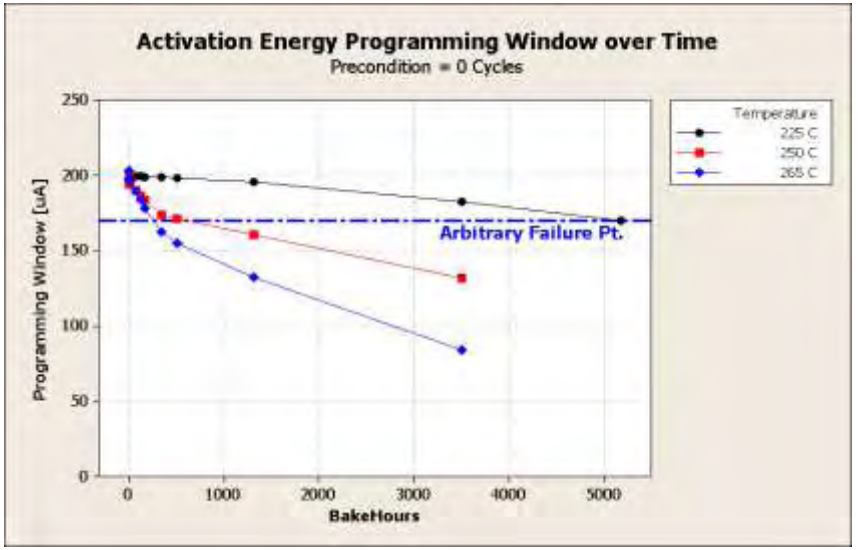
Not always…

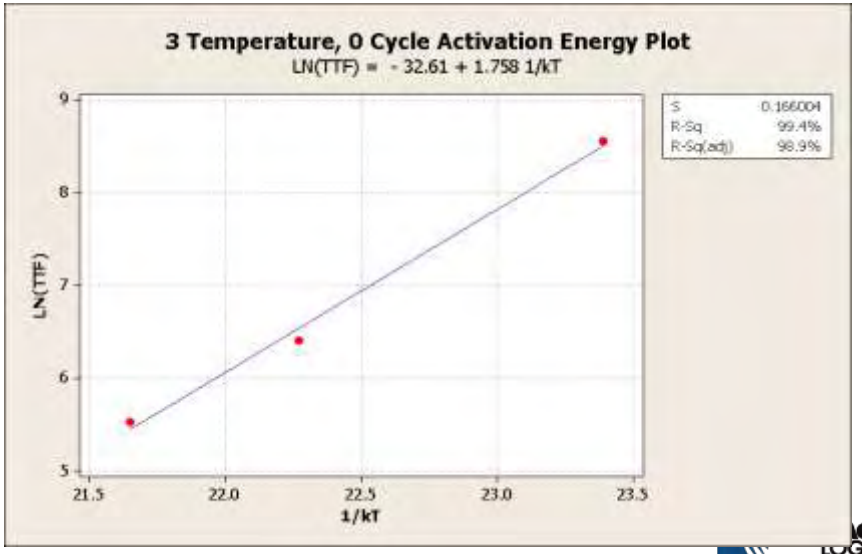
NVM Reliability Concerns

- Data retention (intrinsic)
  - Ability of a process to retain charge
- Endurance
  - Ability of high voltage devices to sustain stress
  - Gate oxide degradation (trap-up)
- Write disturb
  - Unselected rows cumulative stress
- Tail bits
  - Enhanced leakage caused by defects and / or cycling
- Conclusion : passing Qual is only a stepping stone to guarantee reliability for the most stringent applications (e.g. automotive)

Intrinsic Retention

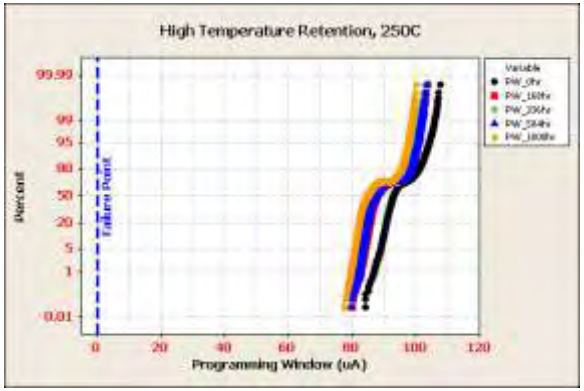
- Inherent ability of each bit (floating gate) to retain charge
  - Highly accelerated by temperature
  - Follows the Arrhenius model with a process dependent activation energy
- Validation Methodology
  - Extract activation energy
    - Monitor cell current drift vs. time and bake temperature
    - Ea > 1eV is typical for FG NVM
  - De-rate extended bake test condition to use model



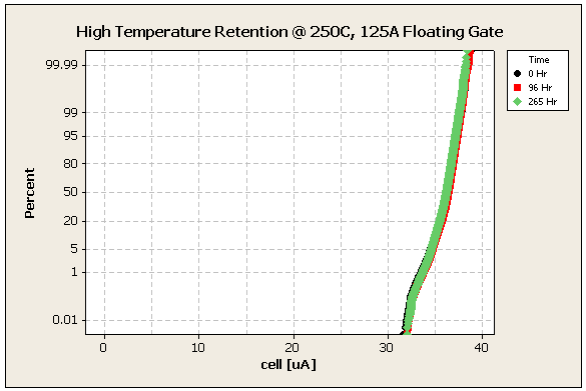


Intrinsic Retention vs. Gate Oxide

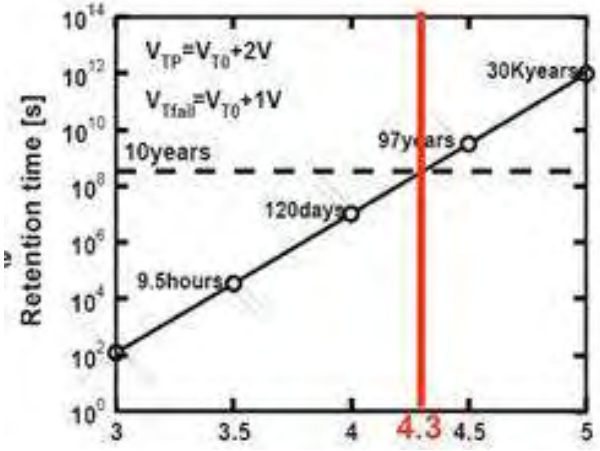
2.5V Oxide (~50Å)



5V Oxide (~125Å)



Literature

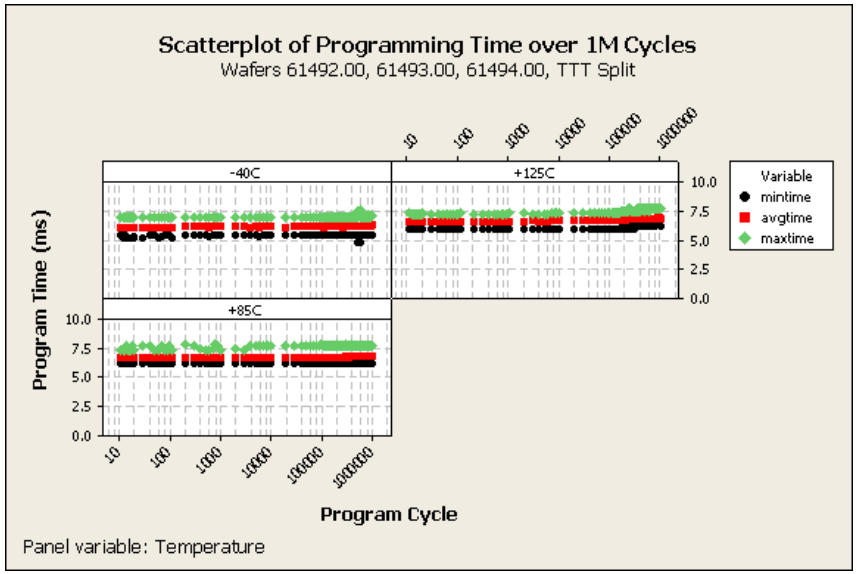


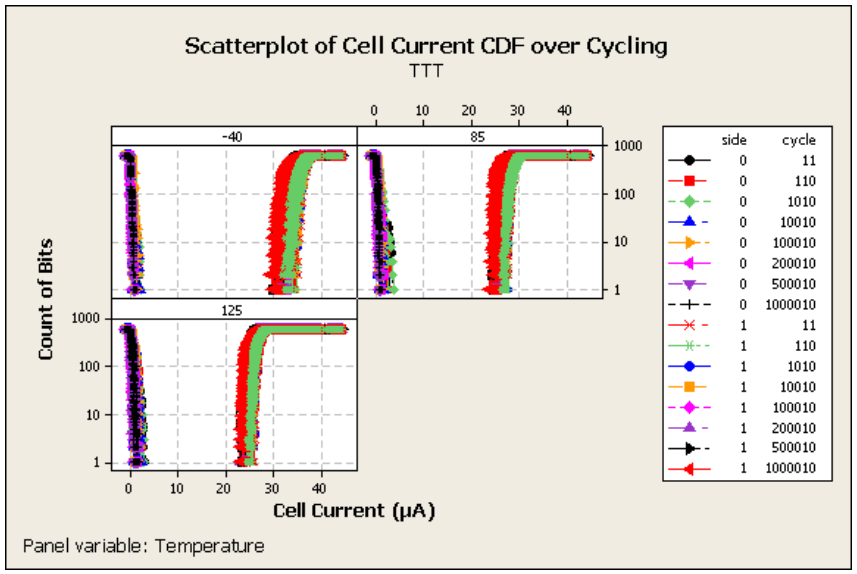
Recent developments on Flash memory reliability
D. Ielmini et al

- Excellent intrinsic retention obtained with Tox ranging from ~50Å (65nm) to ~125Å (.25um 5V)
  - Extended 250C retention bake equivalent to **>> 10 years @ 150C** regardless of oxide thickness
- Theoretical paper by D. Ielmini suggest 43A is limit for Tox and 10 years of intrinsic retention

Endurance

90nm 3.3V

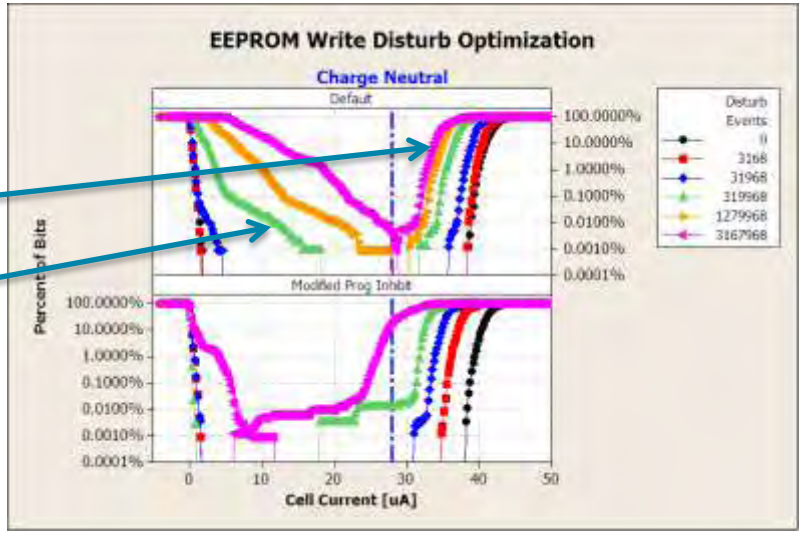


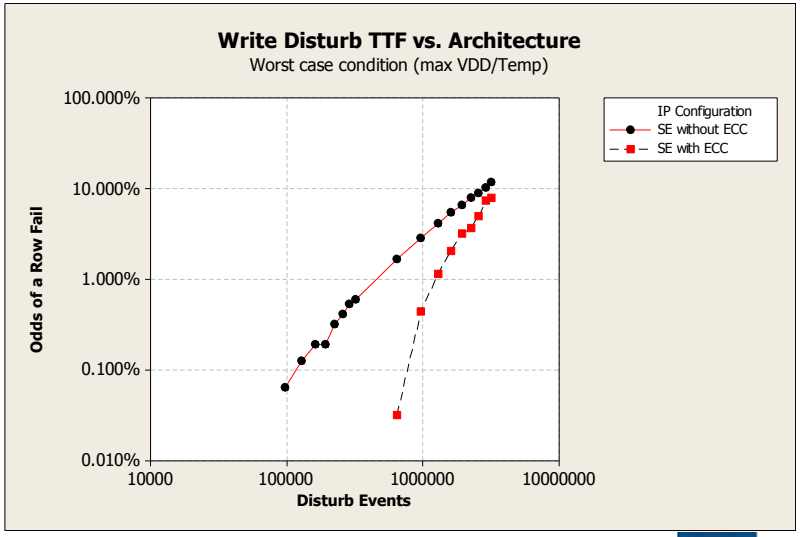


- Endurance margin to spec evaluated by cycling to failure or 10x specification
  - Prog time, programming window monitored during experiment
- Results obtained on key nodes demonstrate **1M cycles** capability across temperature with zero failure

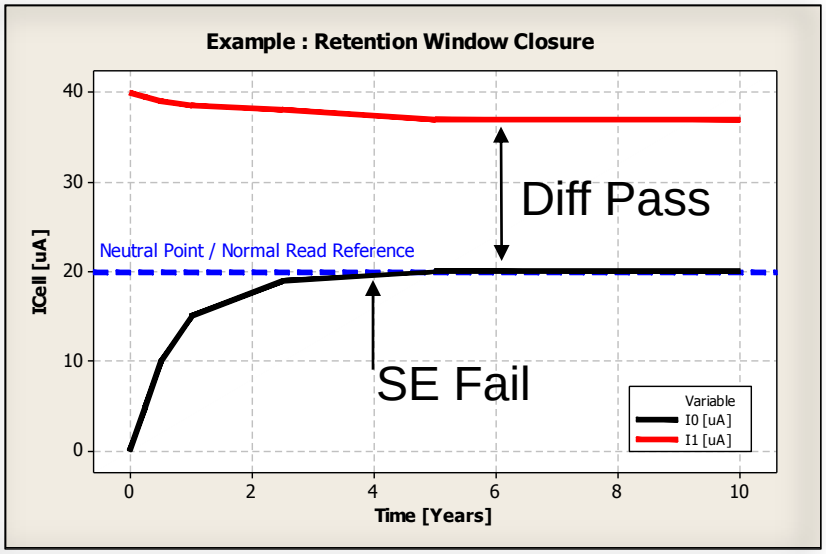
Write Disturb

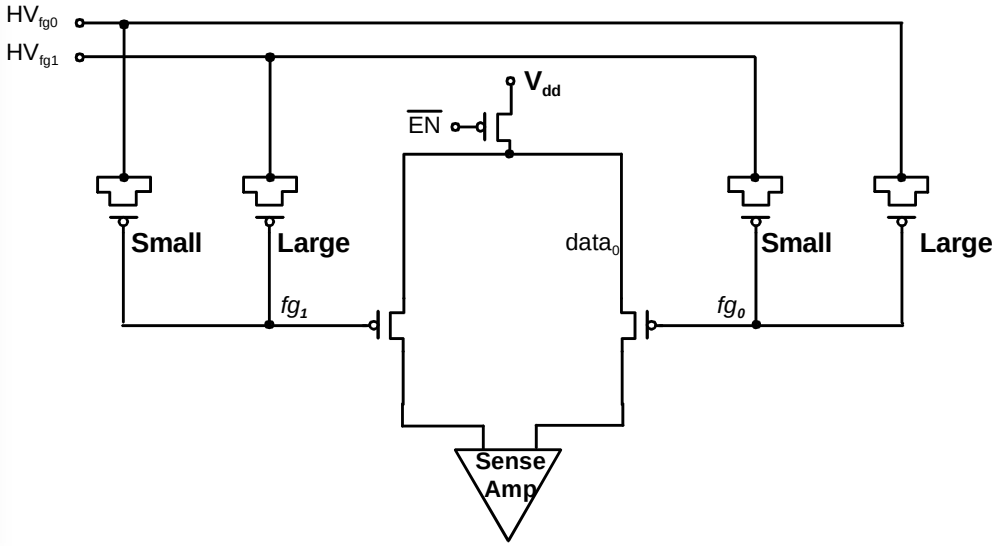
- Un-selected rows are being disturbed during programming
  - Main distribution charge loss
  - Tail bits (i.e. fast disturb bits)
- Centering Prog Inhibit voltage critical to maximize reliability performance
  - Straddle neutral point = best
- Using ECC can significantly improves write disturb immunity by correcting the tail bits





Tail Bit – Reliability vs. Architecture

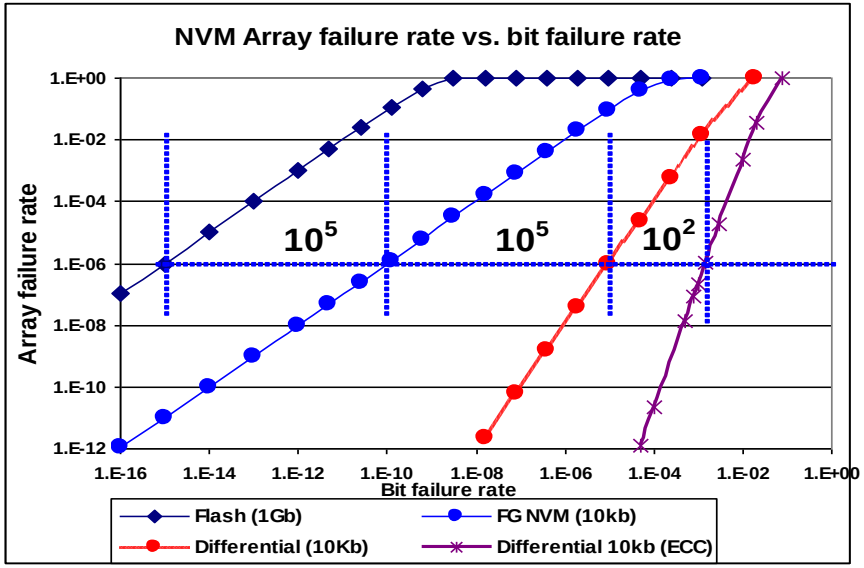




- Tail bit = Floating Gate that looses charge faster than main distribution
- Retention failure → a floating gate (bitcell) lost its charge and the information is lost
- Architectures can compensate for some tail bits
  - Error Correction Code (ECC)
  - Differential bit (redundancy)
  - Combination of the above
- Virage Logic differential bitcell is **intrinsically reliable** against defect / tail bits providing a measure of **fault tolerance**

Tail Bit – Reliability vs. Architecture (theory)

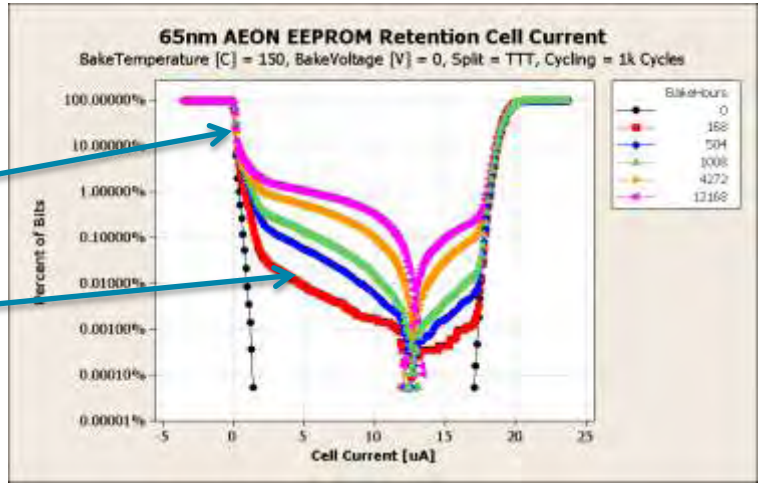
- Redundant non-volatile bitcells are inherently reliable
  - Fails if and only if all Floating Gates fail
  - If Floating Gate failure rate = f
    - Differential bitcell failure rate ≈ $(f)^2$
    - Quad bitcell failure rate ≈ $(f)^4$
- Error Correction Code
  - Further increases reliability
- Combining redundancy and ECC allows VIRL to design a reliable NVM with a high % of tail bits
  - Redundancy scheme and/or error correction depends on probability that a FG fails
  - Tolerates very high failure rate
  - Easy to demonstrate that minimum requirement is met (< 100k bits needed)
  - 0.1% FG failure rate → array still meets < 10 ppm reliability!

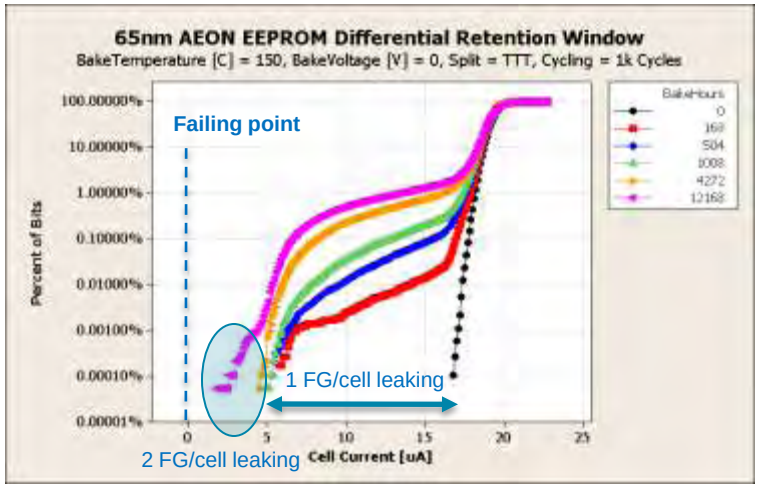


Architecture	Arbitrary FG Failure rate	PPM (2k bit)	Market
SE	0.1%	~850,000	None
SE + ECC	0.1%	~42,000	None
Differential	0.1%	~2,000	Consumer
Differential + ECC	0.1%	<0.05	Automotive

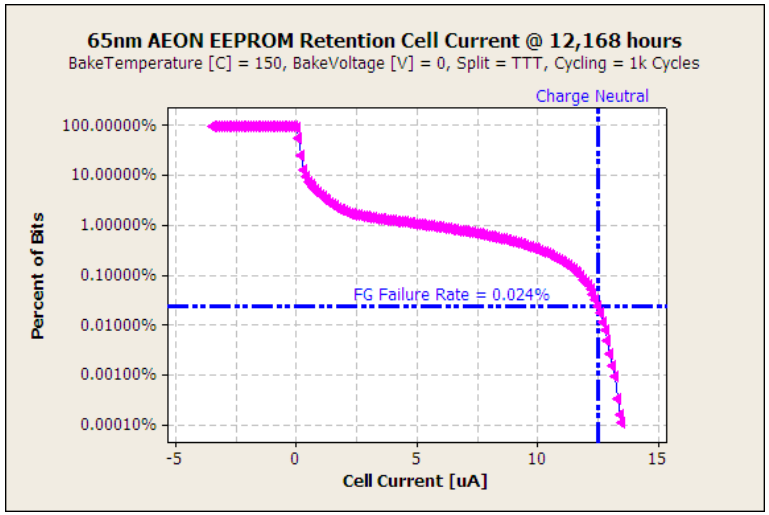
Extended Retention Bake with 2.5V Oxide

- 65nm AEON EEPROM
  - 2.5V I/O Gate oxide (~ 50Å)
  - >12,000 hours of bake @ 150C
    - No intrinsic retention shift
    - Large number of tail bits leaking towards charge neutral (~12.5uA) over time
- Programming window (|i1-i0|) is key retention metric for differential bitcell
  - PW ≈ 0uA → failure
  - PW remains > 0uA
    - Zero differential bit failures
    - < 0.001% of differential bitcells have both floating gate leaking (easily handled with ECC)
- Excellent retention performance for 65nm AEON technology despite large number of tail bits





Retention Results : Does it Fit the Model?



Architecture	FG Failure rate	# Rows tested	# Rows failing (Model)	# Rows failing (Data)
SE	2.4E-4	48604	364	386
SE + ECC	2.4E-4	48604	1.88	2
Differential	2.4E-4	48604	0	0
Differential + ECC	2.4E-4	48604	0	0

- Digital read failures tallied as a function of the architecture (reads performed in single ended or differential mode and with or without ECC)
- Theoretical number of failing rows calculated based on
  - Total number of rows tested (48,604)
  - Floating Gate Failure rate after 12,000 hours of bake estimated from cell current data (2.4E-4)
- Excellent match between model projection and digital reads
  - Validates that FG failure rate is key metric
  - Validates inherent robustness of differential bitcell approach to handle tail bits

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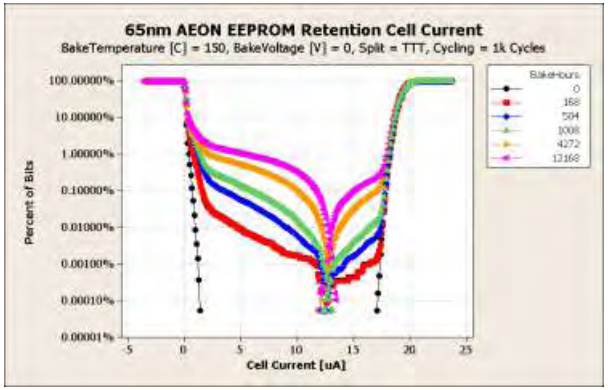
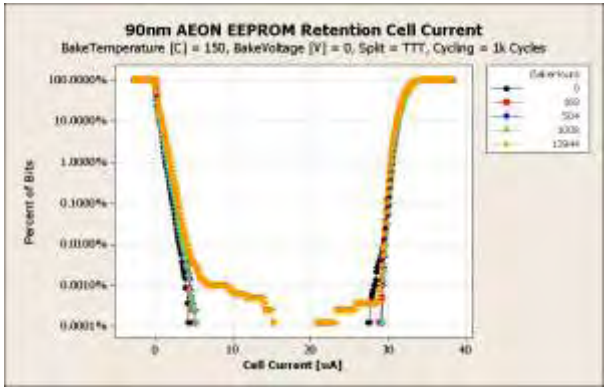
Retention Results : FG Failure rate vs. Process

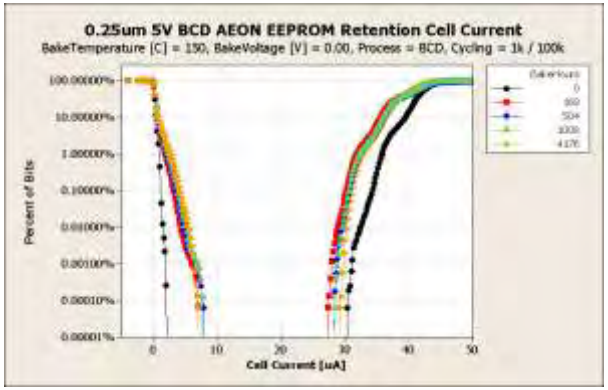
65nm (~50Å)



90nm (~70Å)



250nm (~125Å)



Technology	Tox (Å)	Estimated FG Failure Rate (%)	SE (PPM)	SE + ECC (PPM)	Diff (PPM)	Diff + ECC (PPM)
65nm LP	~50	0.4	1,000,000	930,000	122,000	50
90nm LP	~70	0.001	79,000	18	< 1	~0
0.25um 5V	~125	<0.00003	< 2,400	<< 1	<< 1	~0

- 2.5V I/O oxide → Differential + ECC architecture = consumer / industrial reliability
- 3.3V I/O oxide → Differential (with/without ECC) = automotive reliability
- 5V I/O oxide → Single Ended + ECC or Differential = automotive reliability

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Conclusions

- Highly reliable CMOS NVM IP is available on nodes ranging from 0.25um 5V down to 65nm
- Manufacturability validated by testing IP on process splits beyond operating window
- Quality demonstrated by exceeding qualification standards and performing a knowledge base qualification flow
- Extended Reliability studies on data retention, endurance and disturb guarantee highest quality level

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