Progress and Prospect for MRAM

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Everspin Introduction

• Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor
• The leading developer and manufacturer of integrated magnetic products
  • Industry-first MRAM supplier since June 2006
• Current MRAM products
  • Parallel interface products ranging from 256k-16Mb
    • Infinite endurance, >20 year data retention, 35 ns read & write speed
  • Serial interface products ranging from 256kb-1Mb
    • 40 MHz SPI interface, No write delay, infinite endurance
Everspin MRAM Technology

- Simple 1 transistor + 1 MTJ memory cell
- Data stored in magnetic polarization, not charge
- State of bit detected as change in resistance
- Always non-volatile
- Non-destructive read, unlimited endurance
- Leverage CMOS semiconductor ecosystem
- Everspin - “Electron spin is forever”
Memory Endurance vs. Cycle Time

- **Write/Program Cycle Time (s)**
- **Endurance (Cycles)**

- **HDD**
- **NAND**
- **NOR**
- **SRAM**
- **Code Storage**
- **Data Storage**
- **Working Memory**

- **FeRAM**
- **PRAM**
- **NOR**
- **RRAM**

- **Non-volatile**
- **Volatile**

Flash Memory Summit
MRAM bit switching

**Toggle-MRAM**
- **in production**
  - Cross-point architecture
  - Current along bit line and digit line to switch at intersection

**ST-MRAM**
- **in development**
  - Current $I_{DC}$ flows through MTJ and transistor
  - Fixed magnet polarizes $I_{DC}$
  - Spin-transfer torque programs free magnet
    - Conservation of angular momentum

**Diagram Notes**
- Bit line write current
- Free magnet
- Tunnel barrier
- Fixed magnet
- Isolation transistor
- H-field
- Conservation of angular momentum
Spin Torque MRAM

Use spin momentum from current to change direction of $S, m$.

$\Delta S \over \Delta t = Torque$

Graph showing resistance ($\Omega$) vs. current (mA) with $R_{\text{max}}$ and $R_{\text{min}}$.
Low Switching Current

- Demonstration of low write current with 60nm bits
- Energy barrier = 60kT

Measured on 16kb CMOS array
Large Separation of $V_{sw}$ and $V_{bd}$

16kbit integrated CMOS arrays

- Excellent separation $\approx 20\sigma$, due in part to $\sigma_{sw} \approx \sigma_{bd} \approx 4\%$
Scaling ST-MRAM

- Today: Reduce $J_c$ for reliability and smaller transistors
- Continued scaling: maintain energy barrier and manage resistance distributions

- ST-MRAM bits scale favorably to available current from transistor
  - Low $J_c$ for reliability is the bigger issue
- Continued scaling requires innovative magnetic devices and materials
  - Enhanced energy barrier
  - Increased TMR

$I_c$ calculated for $J_c=2\text{MA/cm}^2$
Summary

- MRAM is a highly reliable, high-performance, nonvolatile memory IC, with unlimited endurance.
- MRAM has the unique characteristics of a working memory while providing non-volatility.
- Current MRAM product densities range from 256kb-16Mb.
- Higher density MRAM products in development will utilize Spin Torque switching and will maintain MRAM’s unique characteristics.