



NAND Flash Scaling is EZ

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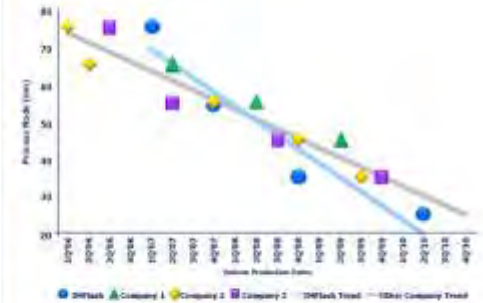
NAND Scaling

- NAND Scaling continues at a relentless pace
- Recent pace exceeds the long-term semiconductor industry trend
- NAND Flash now represents the most advanced semiconductors in the world
- Approaching the atomic level where storage levels are separated by a countable number of electrons

Micron NAND Process Migration

Micron is a full technology generation ahead of the competition.

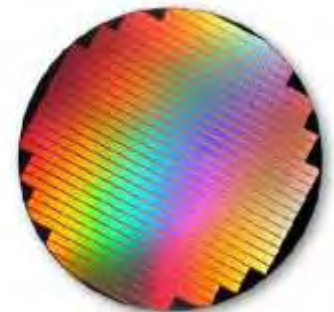
Semiconductor Insights recognized our innovation in 34-nanometer NAND flash technology as the "Most Innovative Process Technology"



Micron 25nm NAND Represents the World's Most Advanced Semiconductor Process Technology

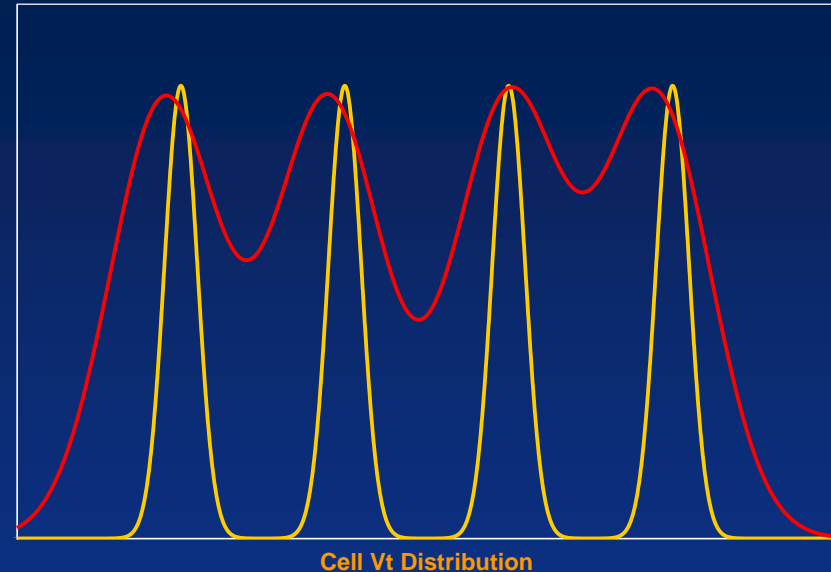
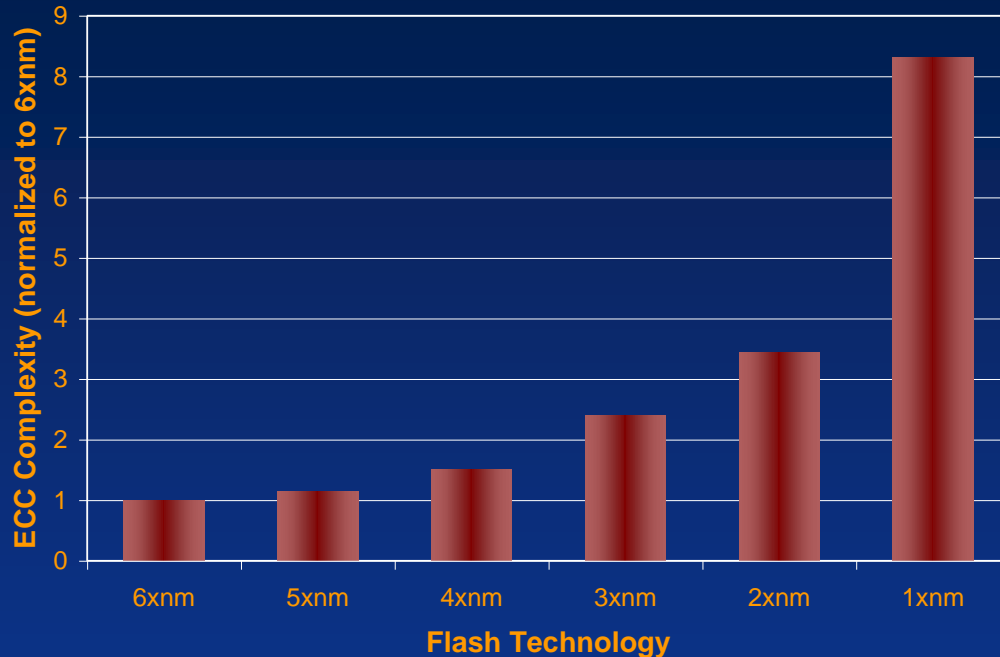


64Gb MLC Die at 167mm²



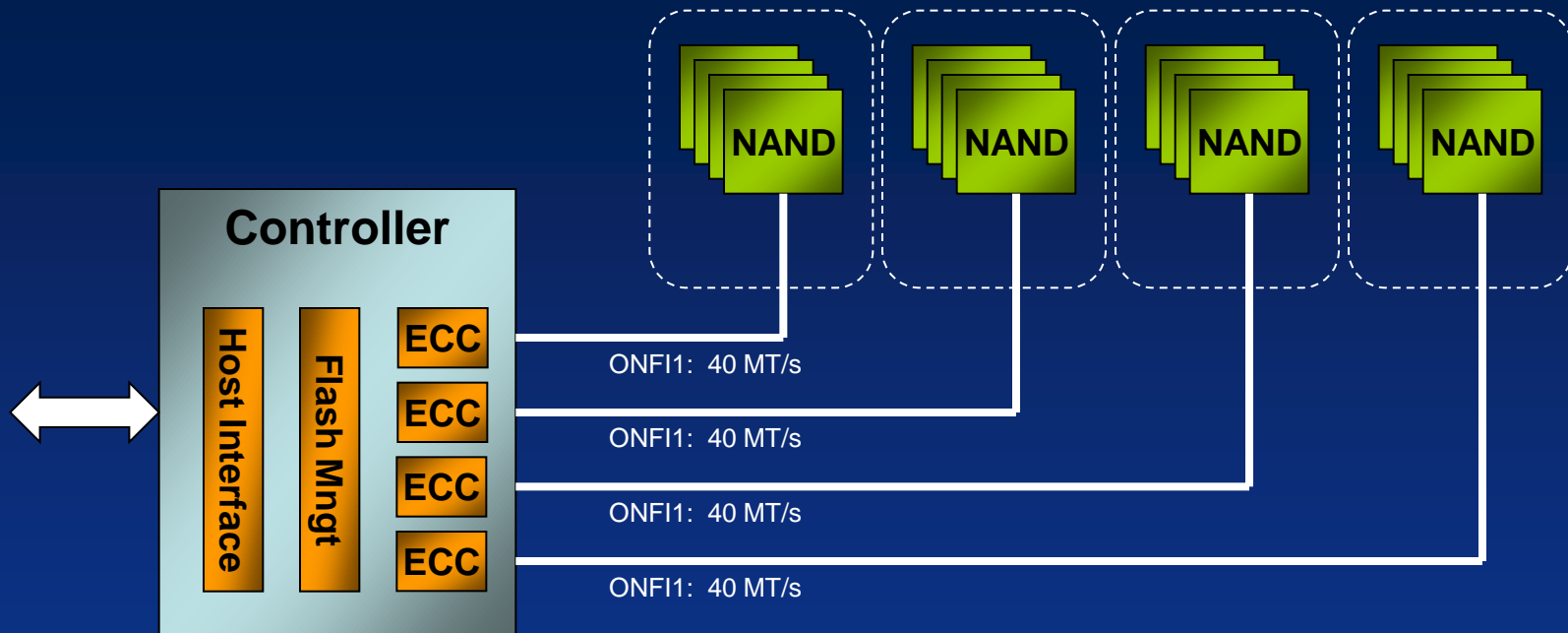
>3TB of storage per wafer

NAND Scaling Complexity



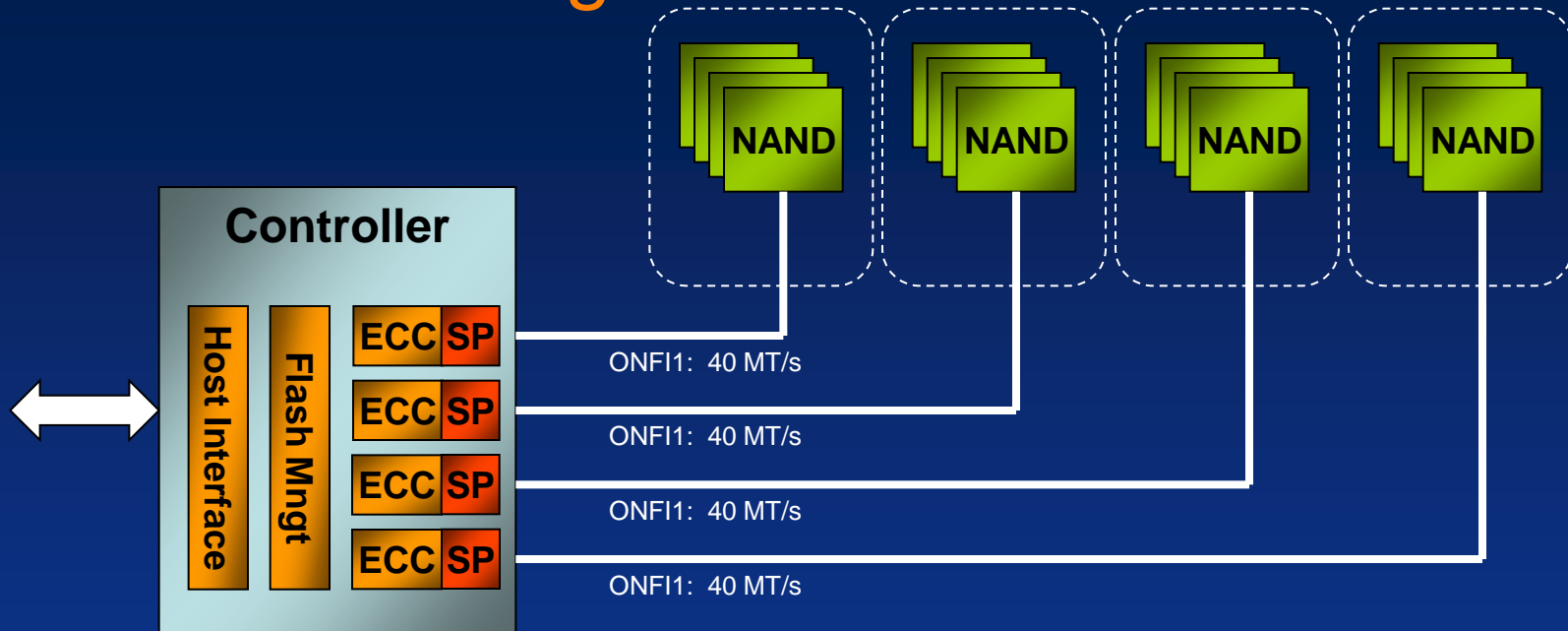
- Increasing complexity – ECC requirements have been increasing for years
- Signal management has long been key to Flash reliability, but no longer contained at the interface boundary

Traditional System Architecture



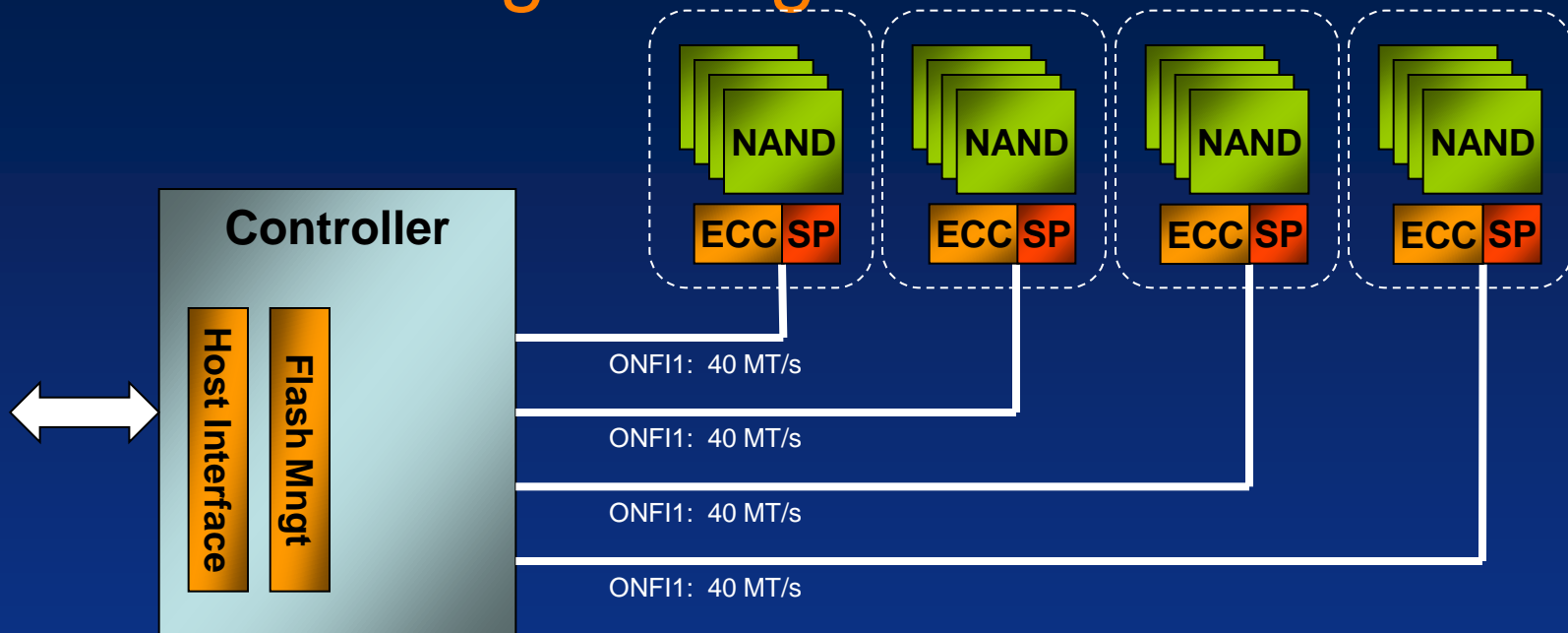
- Most systems using NAND have architectures similar to this
- ECC sized to support target suppliers across a range of technology nodes
- Controller must be sized for maximum capacity and performance; product SKUs can be de-featured from there

Traditional System Architecture – Growing Dilemma



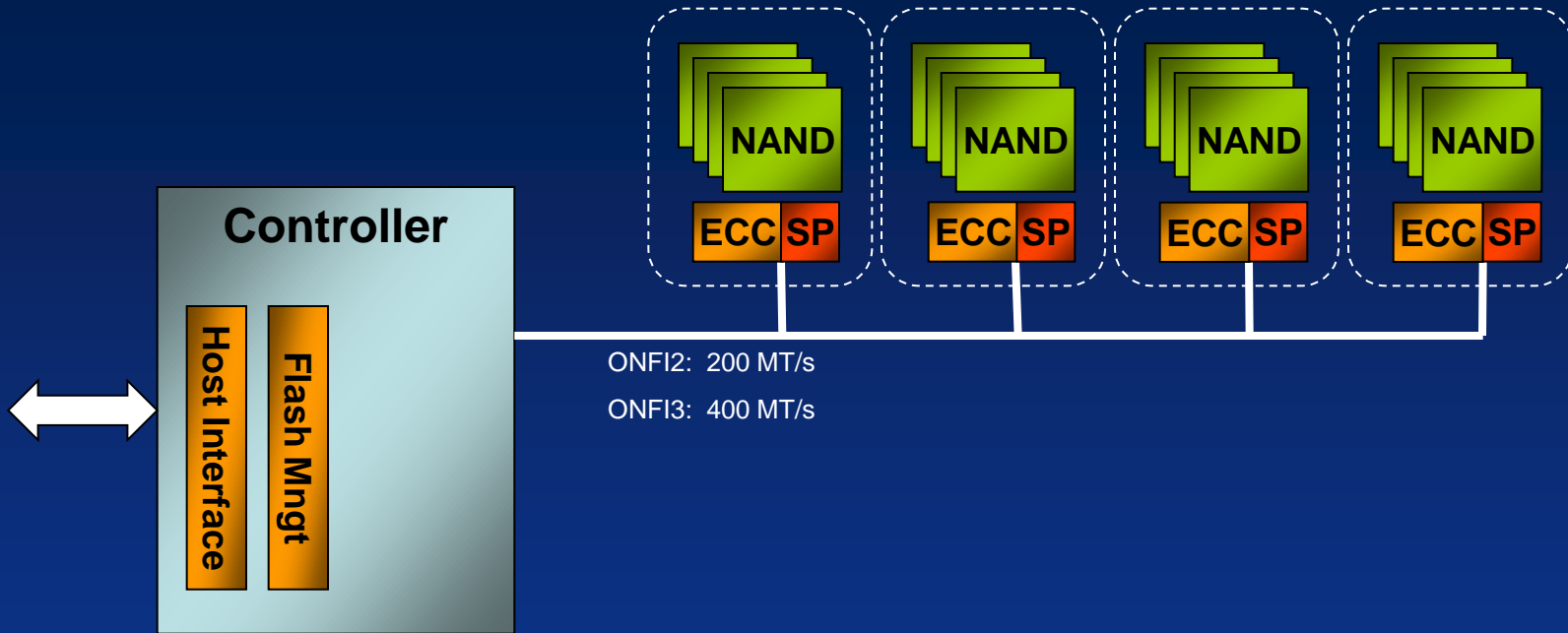
- Growing signal processing requirements and ever-increasing ECC creates controller implementations more tied to Flash technology than ever
- ECC+SP can dominate the controller gate count, and the pin requirements can impact die size and package selection

Emerging Architecture – Abstracted Storage using EZ-NAND



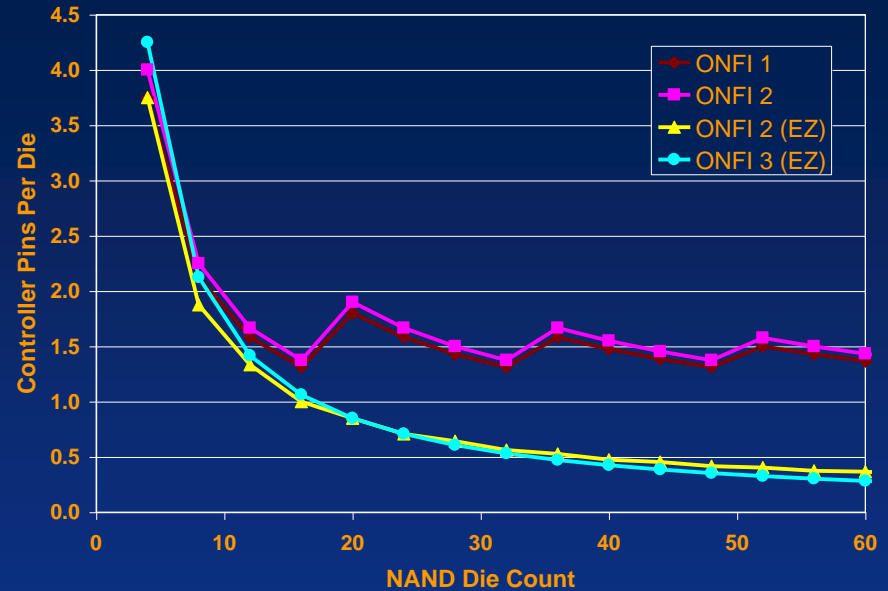
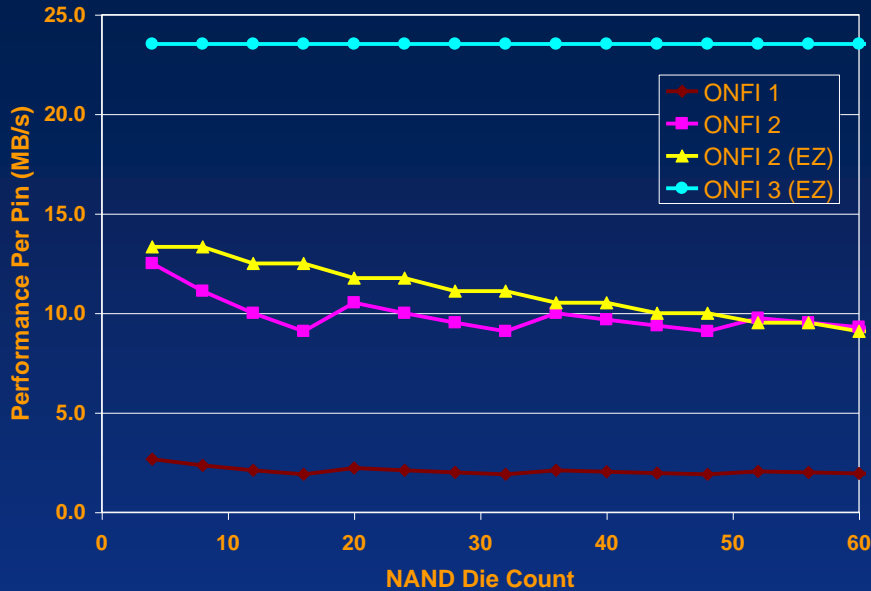
- Tightly coupling the ECC and signal processing ensures error management is precisely tuned for the NAND technology
- Controller ASIC becomes independent of Flash technology
- More scalable across capacity SKUs; system doesn't include more ECC+SP than is required

Emerging Architecture – Higher Bus Performance



- High bus speeds and the EZ-NAND controller combine to increase the capacity and performance per pin on the controller
- Controller costs are minimized

Host Architecture Impact



- ONFI3 and EZ-NAND provide increased performance, while also dramatically decreasing controller pin counts
- No longer does higher capacity require ever-increasing controller resources
 - 1/3 of the controller pins and nearly 3x the performance



Summary/Conclusion

- NAND scaling continues relentless pace
- Architecture changes are required, but system benefit is significant
 - Simpler controllers with fewer gates
 - Fewer pins and the promise of real technology-independent Flash management
- EZ-NAND and ONFI3 offer significant benefits to controller and system architectures