NAND Flash Trends for SSD/Enterprise

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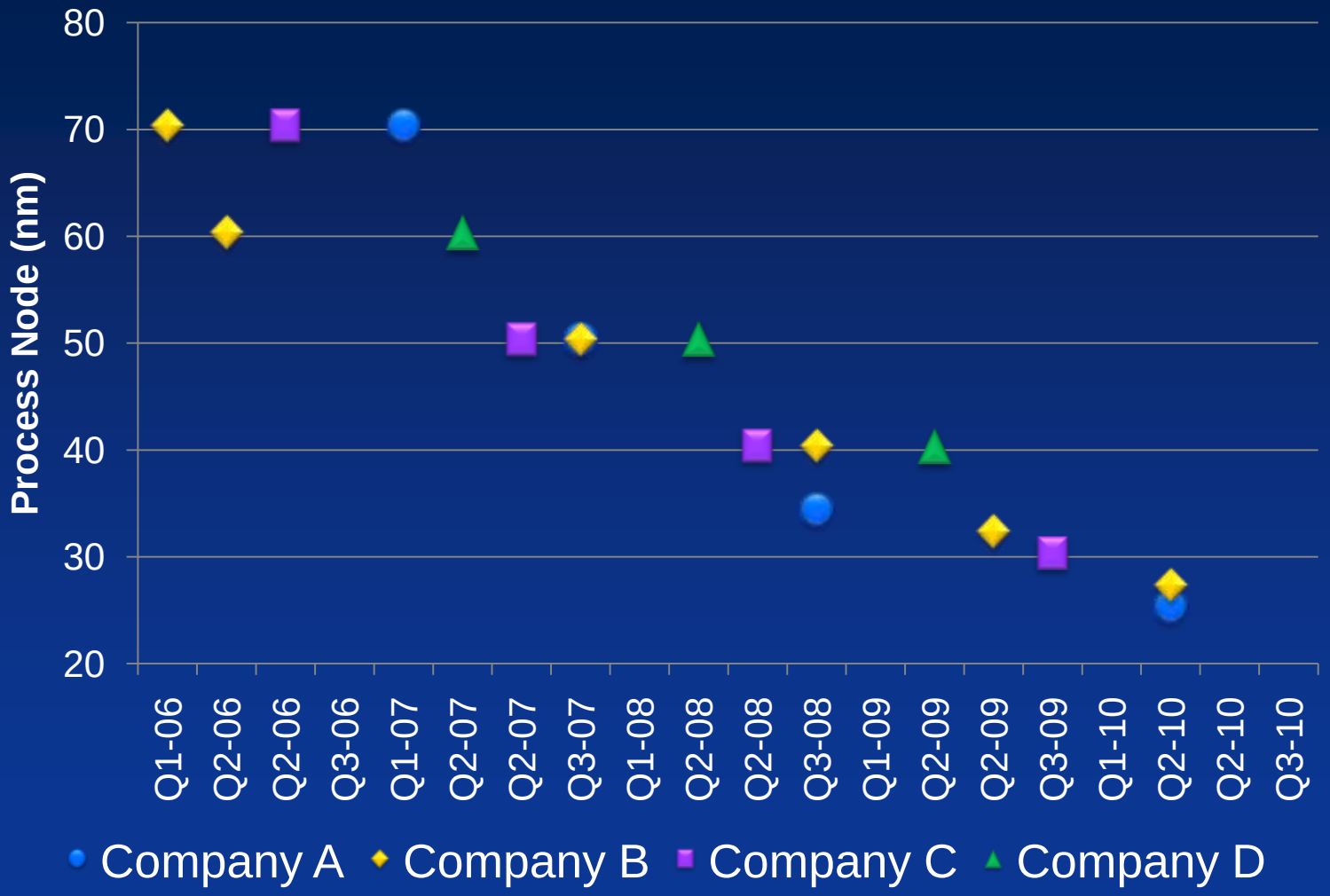
Abstract

- NAND Flash is the nonvolatile memory behind SSDs. It is also being adopted in the enterprise workspace traditionally owned by hard disk drives and DRAM.
- In its relentless pace to reduce cost, NAND has been shrinking faster than Moore's Law.
- With this rapid pace, NAND Flash architecture – page sizes, block sizes, and ECC requirements – has significantly increased.
- This presentation takes a fairly technical look at where NAND Flash has been, where it's at today, and where it is going in the next 2-3 years.
- It looks specifically at the trends in architecture (page size, block size), interface (20 to 400MB/s), performance (sequential and random), and reliability (ECC, data retention, cycling) with emphasis toward adoption in SSD and enterprise applications.
- Finally, as NAND Flash is going through these significant transitions, this presentation covers not only what you need to do to prepare, but also what NAND Flash vendors are doing to prepare for the future to make sure that this memory can continue to be used in future applications.

Topics

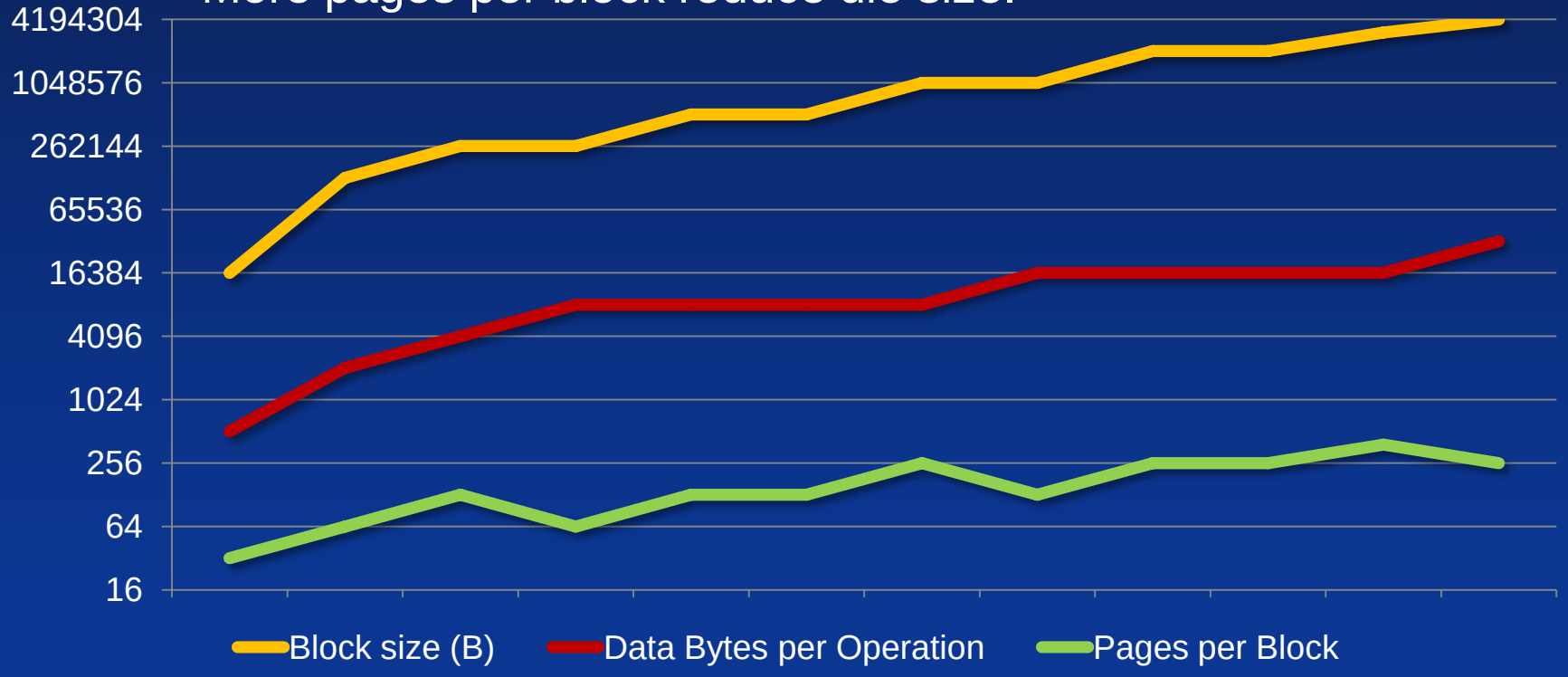
- NAND Flash Trends
- SSD/Enterprise Application Requirements
- A Look to the Future

NAND Process Migration: Shrinking Faster than Moore's Law



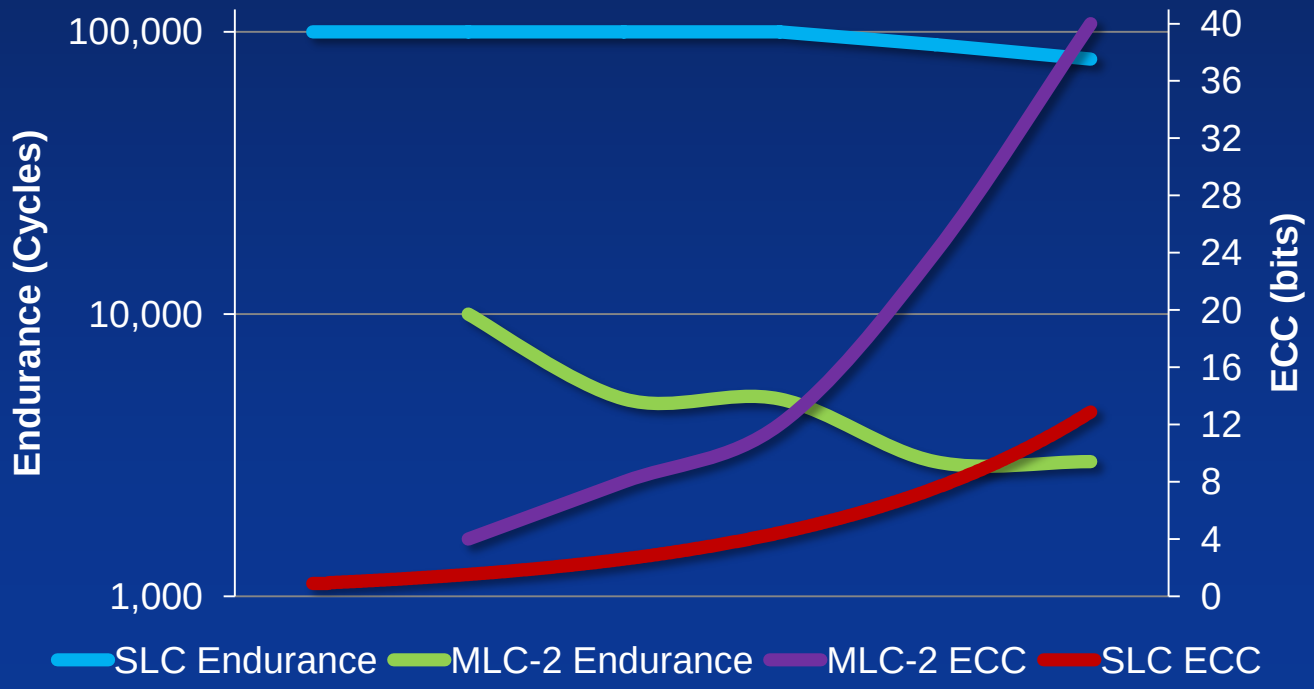
Memory Organization Trends

- NAND block size is increasing.
  - Larger page sizes and more planes increase sequential throughput.
  - More pages per block reduce die size.



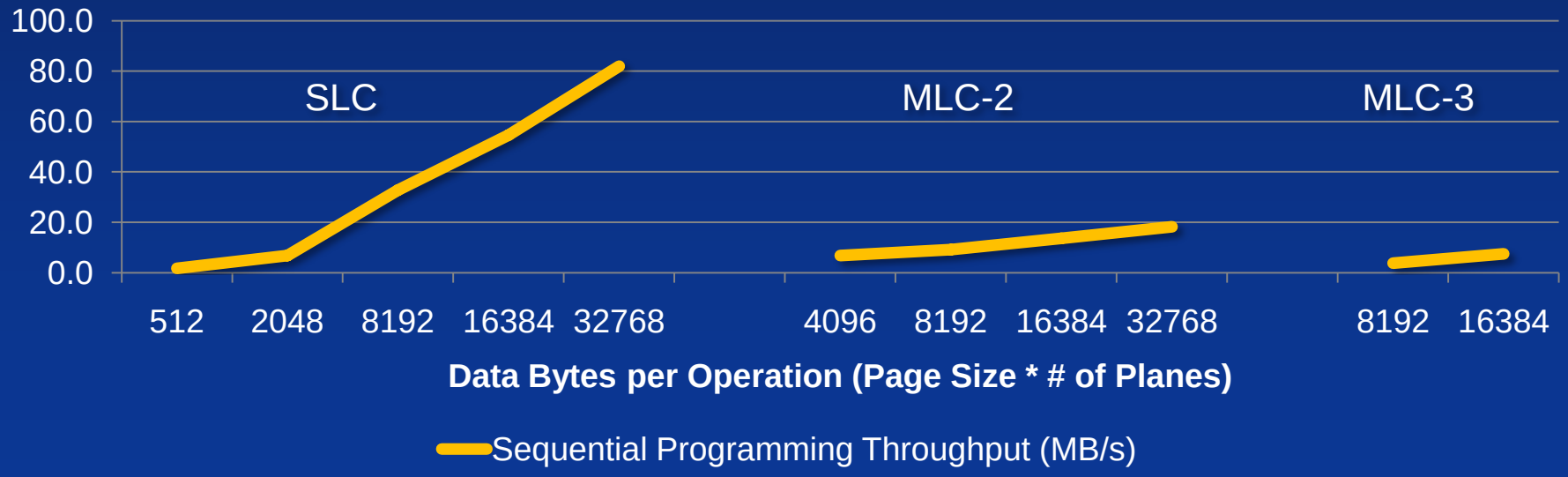
Consumer-grade NAND Flash: Endurance and ECC Trends

- Process shrinks lead to less electrons per floating gate.
- ECC used to improve data retention and endurance.
- To adjust for increasing RBERs, ECC is increasing exponentially to achieve equivalent UBERs.



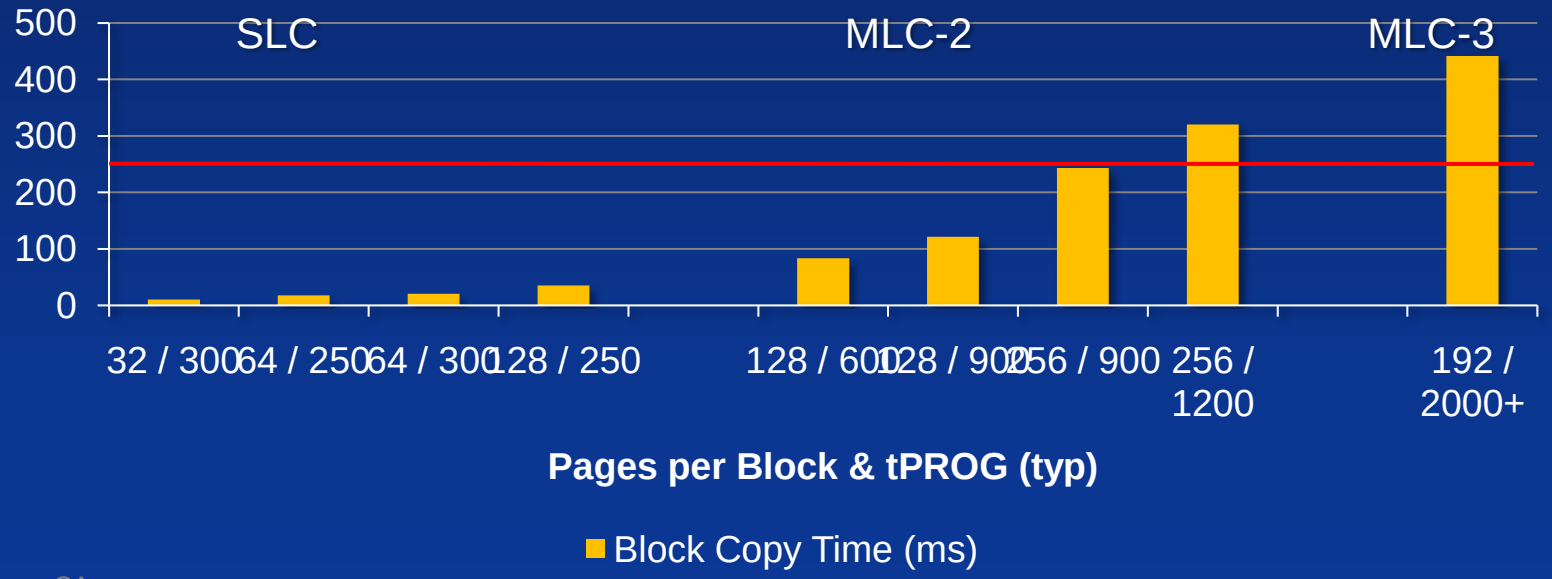
Larger Page Sizes Improve Sequential Write Performance

- For a fixed page size, write throughput decreases as NAND process shrinks
- NAND vendors increase the page size to compensate for slowing array performance
- Write throughput decreases with more bits per cell



More Pages Per Block Affect Random Write Performance

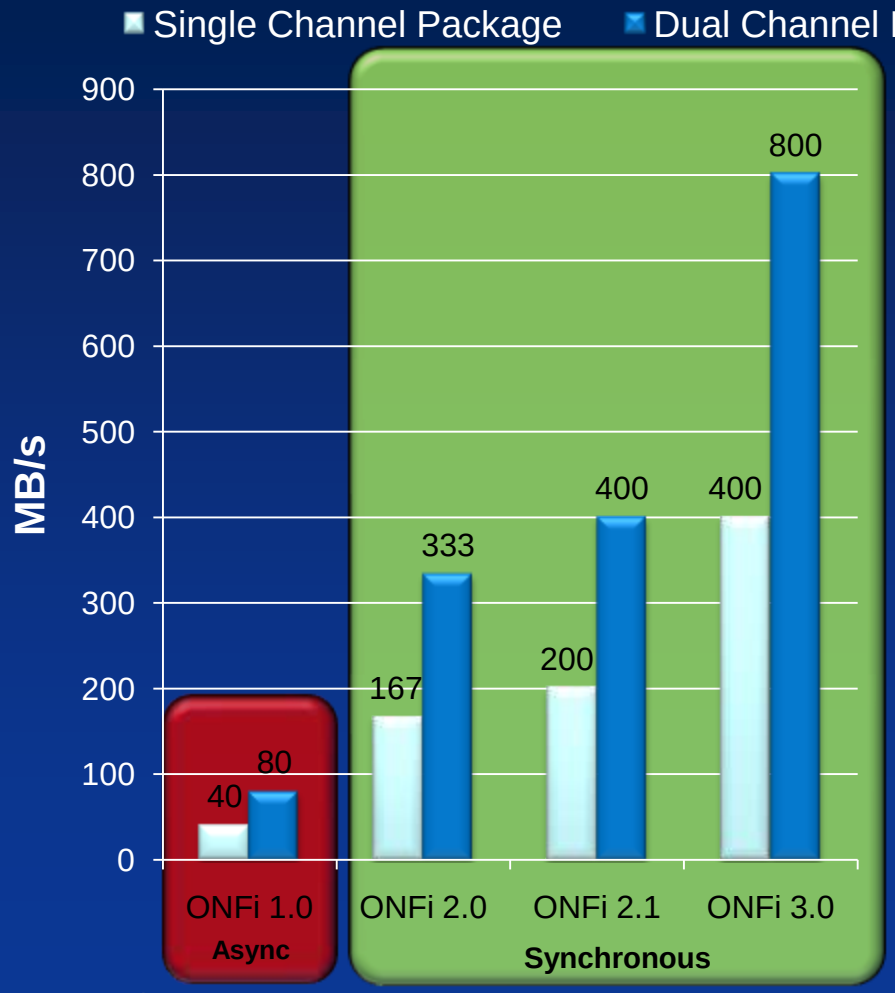
- The block copy time is the largest limiting factor for random write performance.
- As block copy time increases, random performance decreases.
  - Number of pages per block is the dominant factor.
  - Increase of tPROG is the next largest factor.
  - Increase in I/O transfer time due to increasing page size (effect not shown below) is also a factor.
- Some card interfaces have write timeout specs at 250ms, which means that block management algorithms manage partial blocks.



NAND Interface Trends

Interface Standard (x8)	Max Throughput (MB/s)
No standard	40
ONFI 1.0 Async (12/06)	50
ONFI 2.0 Sync (2/08)	133
ONFI 2.1-2.2 Sync (1/09, 9/09)	200
Toggle Mode (not yet published)	200
ONFI 3.0 Sync (2010)	400

The ONFI Advantage



- Supports simultaneous read, program, and erase operations on multiple die on the same chip enable since ONFI 1.0
- Only industry-standard NAND interface capable of 200MB/sec data rate from a single die
- Two independent channels in a single package (doubles the bandwidth)
- In volume production today
- ONFI 3.0 wrapping up this year to bring interface throughput to 400MB/s

SSD/Enterprise vs. Consumer Applications

- SSD/Enterprise applications are different than typical consumer applications in several ways
  - Higher total system density
  - More throughput required, including in random operations
  - Fixed data sizes – e.g. database: 4KB or 8KB
  - Higher endurance/reliability requirements
  - More consistent use over time

Meeting SSD/Enterprise Application Requirements

Application Requirement	Controller	SSD/Enterprise-grade NAND Flash
Higher system density	Ability to handle many NAND Flash – some controllers up to 256 die	
More throughput	Page-based block management, DRAM cache, Overprovisioning, More I/O channels, Faster I/O channels, Multiple ECC engines, Simultaneous operations	Faster I/O channel

Meeting SSD/Enterprise Application Requirements, Part 2

Application Requirement	Controller	SSD/Enterprise-grade NAND Flash
Higher endurance / reliability	Higher ECC	More ECC required, Lower UBER, More endurance
More consistent use over time	Balanced block management to reduce write amplification	

SSD/Enterprise-grade NAND Flash

- Higher Endurance
  - Achieves higher endurance than consumer-grade NAND Flash
- Lower Data Retention at Max Endurance
  - No change to data retention at time 0
  - Enterprise applications tend to use NAND more consistently over its lifetime, so data retention *at max cycling* becomes less important and is reduced

SSD/Enterprise-grade NAND Flash, Part 2

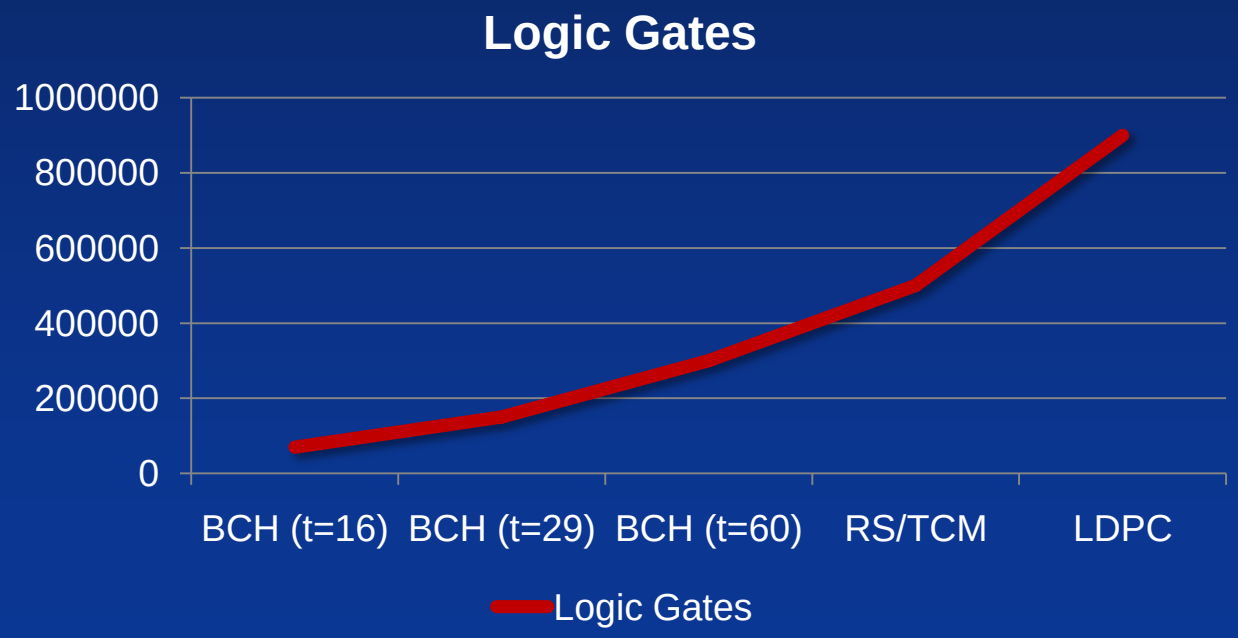
- ECC tuned for lower UBER
  - Providing more ECC to a consumer-grade NAND Flash does not necessarily improve endurance
  - SSD/Enterprise-grade NAND Flash is tuned to improve endurance while reducing UBER, requiring more ECC
- Modest performance
  - NAND array performance is modestly slower than consumer-grade NAND Flash
  - Controller helps achieve better system throughput through more channels, faster interface speeds, overprovisioning, higher parallelism

SSD/Enterprise-grade NAND Flash, Part 3

- Fast I/O Interface
  - Allows better utilization of I/O channels – higher bandwidth
  - Immediately useful for single die read performance
  - Modest improvement for write performance with multiple die
  - Reduces I/O channels required on controller
  - Support 200MB/s today with 400MB/s coming!

Look to the Future

- ECC is going to continue to increase to the point that it will be a significant amount of real estate on a multi-channel controller



How to Handle Increasing ECC?

- This week ONFI announced the release of ONFI 2.3, which provides ECC support bundled with NAND Flash
- Offloads a function that takes a significant chunk of die real estate from the host
- Targeted today for consumer applications
- ONFI has a history of steady, regular NAND interface improvements
- Look to ONFI for future specifications which make this technology ready for SSD/enterprise applications

Questions?

About Michael Abraham

- Manager of Applications Engineering in the NAND Solutions Group at Micron
- Participates on NAND interface standardization activities
- Covers the technical enablement of NAND Flash memories in enterprise and consumer market segments
- Michael earned a BS degree in Computer Engineering from Brigham Young University.