Non-volatile STT-RAM: A True Universal Memory

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Grandis Inc., Milpitas, California

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Outline

- Grandis Corporation Overview
- Current Flash Challenges
- What is Grandis STT-RAM*?
- Grandis STT-RAM Chip
- Memory Technology Comparison
- Grandis STT-RAM Roadmap
- Summary

*STT-RAM: Spin Transfer Torque Random Access Memory
Grandis Corporation Overview

- **Grandis develops and licenses STT-RAM proprietary NVM solutions**
  - Grandis’ STT-RAM enables a wide variety of low-cost and high-performance memory products at the 45 nm technology node and beyond

- Headquarters: Silicon Valley, California

- R&D Offices: California, Japan, S. Korea

- Strong & broad STT-RAM patent portfolio and know-how
  - 50 Granted U.S. Patents
  - > 46 U.S. Patents Pending

Our mission is to establish Grandis STT-RAM as the #1 choice for memory solutions beyond 45 nm
Grandis Milestones in STT-RAM

- 2002: Grandis files first key patents in STT-RAM
- 2004: Grandis reports world’s first STT switching in MTJs
- 2005: Renesas Technology licenses Grandis’ STT-RAM technology
- 2007: Grandis receives Technology Innovation Award from Frost & Sullivan
- 2008: Hynix Semiconductor licenses Grandis’ STT-RAM technology
  
  Grandis wins large DARPA grant to develop STT-RAM chips

- 2009: Grandis upgrades MTJ Fab to handle 300 mm customer wafers
  
  Grandis awarded 9 key patents, taking U.S.-granted patent total to 48
Grandis Development Partners

Flash Memory Summit

Grandis
Pioneer in STT-RAM Technology

hynix
Good memory

BRIDGING THE GAP
50 YEARS
POWERED BY IDEAS

RENESAS
 Everywhere you imagine.

UNIVERSITY OF
VIRGINIA

GRANDIS
Pioneer in STT-RAM Technology

INLAND EMPIRE JUNIOR COLLEGE

NIST

UNITED STATES
NAVAL RESEARCH LABORATORY

Santa Clara, CA, USA, August 2009
Grandis STT-RAM IP Position

- Strong & broad STT-RAM IP coverage
  - Fundamental patents
  - Practical implementation patents
  - Intensive and in-depth know-how and trade secrets

>96 patents filed, 50 patents granted since 2002

Innovative MTJ materials, stacks and cell architecture

STT-RAM array architecture and memory design

Circuit design and system applications
Current Flash Challenges

- **Flash memory evolution**
  - High capacity and low cost, 2, 3 & 4 bit MLC
  - Large page size, increased resource for block management
  - Aggressive scaling, reduced performance and reliability
  - Meeting endurance target becomes more difficult

  These problems create an opening for an alternative, high density Non-Volatile Random Access Memory

- **Grandis STT-RAM will be the solution within 2 years**
  - Initially, embedded SRAM & low power mobile RAM replacement
  - In medium term, NOR flash & DRAM replacement
  - Ultimately, a storage class memory that can replace NAND & HDD
What is Grandis STT-RAM?

- An evolution in magnetic storage from disk drives to solid-state semiconductor memory
  - Uses spin-polarized current ("spintronics") to write magnetic bits
  - Non-volatile, random-access memory with no moving parts
  - Key building block is the magnetic tunnel junction (MTJ)

Grandis has been the pioneer in STT-RAM development since its founding in 2002
**STT Write Mechanism**

- **Spin-transfer torque writing**
  - Uses spin-polarized current instead of magnetic field to switch magnetization of storage layer
  - Has low power consumption and excellent scalability

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**Diagram**: A diagram illustrating the STT write mechanism, including the spin-transfer torque process and the magnetic tunnel junction (MTJ). The diagram shows the current path through the MTJ, with labels for bit line, word line, selection transistor, source line, storage layer, barrier, and reference layer (spin filter). The resistance vs. current graph and the write current vs. magnetic cell width graph are also included.
STT-RAM Universal Memory

- STT-RAM characteristics
  - Non-volatile
  - Highly scalable
  - Low power consumption
  - SRAM read/write speed
  - Unlimited endurance
  - DRAM & Flash density (6 F2)
  - Multi-level cell capability

STT-RAM uses existing CMOS technology with 2 additional masks and less than 5% cost adder
STT-RAM Scalability

- Compared to conventional MRAM, STT-RAM cuts write current by more than one order of magnitude (>10×)

- STT-RAM write current scales linearly with device area
  - <150 µA write current at 90 nm, <50 µA at 45 nm
STT-RAM Minimum Cell Size

- 6 $F^2$ minimum cell size with shared source line architecture
  - Minimum 1 F gate width transistor can drive 6 $F^2$ cell beyond 45 nm

- Future multi-level cell and cross-point architectures will enable further scaling beyond 6 $F^2$
Grandis STT-RAM Chip

- The most advanced STT-RAM prototype chip in the industry
  - Fully-functional
  - 256 kbit capacity
  - 90 nm CMOS
  - 4 Cu metal process
  - LP high reliability CMOS
  - Write current <200 µA
  - Write/read speed 20 ns
  - Endurance >10^{13}

- Higher density chips at 54 nm & beyond are in development
STT-RAM Resistance Distribution

- Large separation between resistance states and small process distribution provide excellent read characteristics
  - TMR (Tunneling Magnetoresistive) signal ~100%
  - $R_{\text{low}}$ distribution sigma 4% ($1\sigma$), $R_{\text{high}}$ distribution sigma 3% ($1\sigma$)
  - $R_{\text{high}} - R_{\text{low}}$ separation = $20\sigma$
STT-RAM Unlimited Endurance

- Unlimited (>10^{15}) write endurance projected from TDDB tests with stressed voltage and temperature
  - 10^{13} endurance demonstrated to date under real operating conditions
## Memory Technology Comparison

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>Flash (NOR)</th>
<th>Flash (NAND)</th>
<th>FeRAM</th>
<th>MRAM</th>
<th>PRAM</th>
<th>RRAM</th>
<th>STT-RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Non-volatile</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Cell size ($F^2$)</strong></td>
<td>50–120</td>
<td>6–10</td>
<td>10</td>
<td>5</td>
<td>15–34</td>
<td>16–40</td>
<td>6–12</td>
<td>6–10</td>
<td>6–20</td>
</tr>
<tr>
<td><strong>Read time (ns)</strong></td>
<td>1–100</td>
<td>30</td>
<td>10</td>
<td>50</td>
<td>20–80</td>
<td>3–20</td>
<td>20–50</td>
<td>10–50</td>
<td>2–20</td>
</tr>
<tr>
<td><strong>Write / Erase time (ns)</strong></td>
<td>1–100</td>
<td>15</td>
<td>1 μs / 10 ms</td>
<td>1 ms / 0.1 ms</td>
<td>50 / 50</td>
<td>3–20</td>
<td>60 / 120</td>
<td>10–50</td>
<td>2–20</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>$10^{16}$</td>
<td>$10^{16}$</td>
<td>$10^5$</td>
<td>$10^5$</td>
<td>$10^{12}$</td>
<td>$&gt;10^{15}$</td>
<td>$10^8$</td>
<td>$10^8$</td>
<td>$&gt;10^{15}$</td>
</tr>
<tr>
<td><strong>Write power</strong></td>
<td>Low</td>
<td>Low</td>
<td>Very high</td>
<td>Very high</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Other power consumption</strong></td>
<td>Current leakage</td>
<td>Refresh current</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td><strong>High voltage required</strong></td>
<td>No</td>
<td>3 V</td>
<td>6–8 V</td>
<td>16–20 V</td>
<td>2–3 V</td>
<td>3 V</td>
<td>1.5–3 V</td>
<td>1.5–3 V</td>
<td>&lt;1.5 V</td>
</tr>
</tbody>
</table>

Existing products

Prototype
### Intensified interest in STT-RAM

<table>
<thead>
<tr>
<th>Date</th>
<th>Event Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apr. 2008</td>
<td>Hynix licenses Grandis' STT-RAM technology, expects to sample 1 Gbit STT-RAM in 2010</td>
</tr>
<tr>
<td>Jun. 2008</td>
<td>Toshiba announces plans to develop 1 Gbit STT-RAM, expects it to replace DRAM by 2015</td>
</tr>
<tr>
<td>Jun. 2008</td>
<td>Korea Government invests $50M in Hynix, Samsung and local university alliance for STT-RAM development</td>
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<tr>
<td>Oct. 2008</td>
<td>Grandis wins large DARPA grant from U.S. government to develop STT-RAM chips</td>
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<tr>
<td>Oct. 2008</td>
<td>Toshiba presents data from 50 nm perpendicular MTJS, expects STT-RAM to achieve 6F2 cell size (same as DRAM)</td>
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<tr>
<td>Oct. 2008</td>
<td>Samsung presents 512 Mbit STT-RAM in 90 nm process, expects it to replace DRAM at sub-30 nm in 2012</td>
</tr>
<tr>
<td>Dec. 2008</td>
<td>IBM–TDK alliance reports statistical study of MTJs for high-density STT-RAM at IEDM conference</td>
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</table>
Grandis STT-RAM Roadmap

- **Year**: 2010 → 2011 → 2013 → 2015

- **STT write current (µA)**
  - $I_{dsat}$: 8ns, 5ns, 3ns, 1ns
  - $I_{write}$: <30F$^2$, <24F$^2$, <15F$^2$, <8F$^2$, <6F$^2$, <4F$^2$

- **Technology node, Memory cell size**
  - 65nm, 45nm, 32nm, 22nm

- **Market Distinctions**
  - $12B embedded SRAM & NOR Market
  - $85B standalone DRAM & NAND Market
STT-RAM Evolution and Market

- **Tech Node**
  - 54 nm
  - 45 nm
  - 32 nm
  - 22 nm

- **Cell Size**
  - Embedded SRAM: 14F²
  - Automotive: 8F²
  - Mobile Phone: 6F²
  - DRAM: 4F²
  - NOR Flash: 4F²
  - NAND Flash: 4F²

- **Market**
  - $100 B
  - $80 B
  - $40 B
  - $10 B

- **Density**
  - 2010: 64 MB
  - 2011: 1 GB
  - 2013: 16 GB
  - 2015: 256 GB
Challenges for STT-RAM

- Grandis is working with its partners to address key challenges for STT-RAM
  - Proving technology reliability for large scale manufacturing
  - Tuning cell design for different application requirements

- But to fully exploit STT-RAM’s characteristics, a fundamental rethink of computing system architecture will be required
  - STT-RAM can enable revolutionary advances in latency, bandwidth, reliability and power-efficiency for data-intensive applications, and other applications not yet envisaged

The return on investment towards reducing overall system cost and added system functionality well justifies the effort to meet the above challenges
Summary

- Spintronics (spin electronics) is a rapidly emerging field
  - It will have a significant impact on technology in the 21st century

- STT-RAM is the world’s first truly universal, scalable memory technology
  - It will enable a new era of instant-on computers and high-speed portable devices with extended battery life

- STT-RAM has a huge potential market
  - It can replace eSRAM & eFlash, at 45 nm, DRAM at 32 nm, and ultimately replace NAND & HDDs as a storage class memory at 22 nm and beyond

Grandis is the pioneer in STT-RAM with a strong & unique IP position, an experienced and dedicated team, and early partnerships in product development with key semiconductor memory players
Thank You!

Please visit www.GrandisInc.com for more information