HLNAND: A New Standard for High Performance Flash Memory

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Objectives

- Address performance and density requirements of Solid State Drive (SSD)
- Cost effectively serve lower end applications

4 Key Flash Applications

- SSD for HDD Replacement
- Flash Memory Card
- USB Flash Drive
- Embedded Apps

Chart showing Sustainable Bandwidth (MB/s) for different densities (4GB, 8GB, 16GB, 32GB, 64GB, 128GB, 256GB). The graph compares SSD, High-end Flash Card for Prosumer, HD Digital Video, Generic Flash Memory Card & USB Driver, and Compressed Digital Video.
NAND Flash Standards

- Defacto standard for asynchronous NAND Flash established by Toshiba in the early 1990’s
- ONFI 1.0 – formal standard for asynchronous NAND Flash resolving incompatibilities among suppliers
- ONFI 2.0 – evolutionary standard adding source synchronous DDR up to 133MB/s
- HyperLink NAND (HLNAND™) – synchronous DDR ring topology introduced by MOSAID
- RamLink – IEEE standard published in 1996 for DRAM main memory using ring topology

HLNAND™ is a trademark of MOSAID Technologies Incorporated
Memory Interface Comparison

- Code storage
- Low latency operation
- Issue commands during data transfers
- Multi-drop bus
- Limited number of loads

- High latency core
- Long data transfers
- Interrupt data transfer to issue commands
- Multi-drop bus
- Limited number of loads

- High latency core
- Long data transfers
- Interrupt data transfer to issue commands
- Point-to-point daisy chain
- Unlimited number of loads
Conventional NAND Flash Interface

- 8 bit, bidirectional, multi-drop bus
- Asynchronous LVTTL signaling up to 40Mb/s/pin
- Speed degradation with more than 4 devices on bus
- Chip Enable (CE) signal required for each device
- Power hungry 3.3V I/O
HyperLink Interface

- Unidirectional, point-to-point, daisy-chain cascade supporting as many as 255 devices in a ring
- No bandwidth degradation with additional devices
- Device address assigned on initialization
- High speed DDR signaling up to 800Mb/s/pin
- Dynamic link width programmable from 1 to 8 bits
- Low Power 1.8V I/O
HyperLink Features

- HyperLink interface can be applied to any device
  - SLC NAND, MLC NAND, NOR, PRAM, DRAM etc.
  - self identified via configuration registers on power up

- Two modes of operation
  - HL1 supporting speeds up to 266Mb/s/pin
    - parallel distributed clock – no PLL required
    - LVCMOS signaling
  - HL2 supporting speeds up to 800Mb/s/pin
    - Source synchronous clocking – a PLL is required
    - HSTL Class1 signaling – matched output driver - no termination required - zero static power
  - Single device supports both modes by sensing Vref pin

- Optional Vpp supply pin for die cost/power reduction
HyperLink Packet Truncation

- Once packet reaches addressed device the write data payload is truncated
- Simultaneous data transfer possible if write device is upstream of read device
HyperLink Advantages

- **Bandwidth**
  - Point-to-point signaling extends to much higher data-rates than multi-drop bus

- **Power**
  - No termination resistors required
  - Point-to-point I/O drivers are much smaller than multi-drop bus drivers and have significantly lower capacitance
  - Packet truncation at destination device reduces power

- **Scalability**
  - Up to 255 devices in a single ring
HL1 Interface

- DDR signaling up to 266MB/s, no PLL required
- No changes to existing Flash process
HL1 Timing

- CSI/CSO – Command and write data Strobe Input/Output
- DSI/DSO – read Data Strobe Input/Output
- Data bursts can be interrupted by terminating CSI/DSI

\[ w = \text{current link width} \]
HL2 Interface

- Source synchronous DDR to 800MB/s with on-chip PLL
- May require improvement to I/O transistor performance
- Fully backward compatible to HL1
- Fully independent banks
  - Launch any operation (read, program, erase) in one bank regardless of activity in other bank(s)

- Flexible plane operations
  - Variable page size (eg. 2KB, 4KB, 6KB, or 8KB) for read and program operations in one bank

- Page-Pair Erase and Random Page Program in SLC, Partial Block Erase in SLC and MLC
  - Using novel, low stress program scheme
  - More closely match erase and program data size, eliminating un-necessary block copy and garbage collection, improving performance and endurance
# HLNAND Instructions

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<th>Operation</th>
<th>1st Byte</th>
<th>2nd Byte</th>
<th>3rd Byte</th>
<th>4th Byte</th>
<th>5th Byte</th>
<th>6th Byte</th>
<th>7th Byte</th>
<th>8th Byte</th>
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<th>2116th Byte</th>
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DA = Device Address, CA = Column Address, RA = Row Address, X = Bank Number
HLNAND Resources

- Available at hlnand.com
  - Architectural Specification
  - Datasheets
  - White papers
  - Technical papers
  - Verilog Behavioral model
HLNAND Emulation System

- DIMM module using DRAM and FPGA fully emulates 200MB/s HLNAND Flash device
- Available to controller and end product manufacturers for system development and benchmarking
HLNAND Multi-Chip Package

- First generation product using conventional NAND KGD
- Small bridge chip provides HyperLink interface
- Significant performance, density, and power benefits
Enabling the Flash Ecosystem

- MOSAID is developing HLNAND for licensing to semiconductor and system manufacturers.
- MOSAID is an active member of JEDEC promoting Flash standardization.
- HLNAND MCP based on conventional NAND Flash will be available first to serve enterprise applications.
- Monolithic HLNAND providing further performance and power advantages will cost-effectively address all applications.
- Unleash the full potential of Flash technology with HLNAND.