An Introduction to Emerging Memory Technologies

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Agenda

- Overview of Emerging Memory Alternatives
- Near Term Candidates
- Longer Term, Litho Defined Candidates
- Non Litho Defined Candidates
- Conclusions
Overview of Emerging Memory Alternatives

- Near Term Candidates
- Longer Term, Litho Defined Candidates
- Non Litho Defined Candidates
- Conclusions
Flash Invented in mid 1980’s
  • NOR flash evolved from EPROM
  • NAND started as poly-poly erase cell later evolving to present structure

~20 years & 10 Generations of High Volume Production
8+ years & 5 Generations of MLC: 2bit / cell

Volume Production Year / Technology Generation

Source: Intel
Emerging Memory Landscape

Today
- EEpROM
- HDD
- NOR
- NAND
- DRAM
- SRAM

Tomorrow
- Floating Trap
- Metal Gate
- Nano Dot
- Barrier Engineering

Future
- Multi Layer 3D
- 3D Gate

Evolutionary Enhancements

Emerging Alternatives
- FeRAM
- MRAM
- PCM

Focus of Today’s Tutorial

Multilayer 3D
- RRAM
- Bridging/Ionic
- Molecular
- Probe Storage
- e-Beam
Overview of Emerging Memory Alternatives

- Near Term Candidates
  - Longer Term, Litho Defined Candidates
  - Non Litho Defined Candidates
  - For Further Study
## Near-term Candidates for Alternative NVM

<table>
<thead>
<tr>
<th>PCM (Phase Change Memory)</th>
<th>MRAM</th>
<th>FeRAM</th>
</tr>
</thead>
</table>
| **Phenomenon:** Resistance change in amorphous and polycrystalline phases.  
**Method:** Phase change induced by injected current | **Phenomenon:** Resistance change due to magnetic polarity  
**Method:** Polarity of one “plate” pinned while other is switched | **Phenomenon:** Applied voltage changes dipole moment of center atom  
**Method:** data read by sensing displacement current |

Source: Intel
FeRAM

Key Attributes
- 1C + 1 Transistor
- Cell Area: 25F² shipping
- Cell Area: 12-15F² demonstrated

Advantages
- Fast R/W performance
- Low power operation
- Bit alterable (no erase)

Issues
- Scaling path <100 nm
- Destructive read
- Read & Write limited (1e⁶ → 1e¹⁰)
- No path to flash/dram level costs

Source: Intel
Key Attributes
- 1MTJ + 1 Transistor
- Cell Area: 35F² shipping (Toggle)
- Cell Area: 6F² theoretical (STT)

Advantages
- “Unlimited” R/W endurance
- Fast R/W latency (<35 ns)
- Bit alterable (no erase)

Issues
- Scaling path
- Write disturbs, power
- New materials, CMOS compatibility
- No path to flash/dram level costs

Source: Intel
Phase Change Memory (PCM)

Key Attributes
- 1R + 1 select
- Cell Area: 5.5-12\(F^2\) sampling
- Cell Area: <6\(F^2\) demonstrated

Advantages
- Clear scaling path to <20 nm
- Ease of CMOS integration
- Fast, “unlimited” read
- Bit alterable (no erase)

Issues
- Write endurance limited: 1e6 to 1e12
- Write latency vs. DRAM

Source: Intel
## Emerging Alternative Memory Attribute Comparison

<table>
<thead>
<tr>
<th>Key Metrics</th>
<th>PCM</th>
<th>MRAM</th>
<th>FeRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Size</td>
<td>~SBC NOR/NAND (5.5-12F² → &lt;5F²)</td>
<td>Larger (35 F² → 6-16F²)</td>
<td>Largest (32F² → 12-15F²)</td>
</tr>
<tr>
<td>CMOS Integration</td>
<td>Good</td>
<td>Fair to Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>Scaling</td>
<td>Excellent</td>
<td>Fair: current, materials</td>
<td>Poor: materials, 3D</td>
</tr>
<tr>
<td>Read Latency</td>
<td>Fast, ~NOR</td>
<td>Fastest, ~xRAM</td>
<td>Fast, ~NOR</td>
</tr>
<tr>
<td>Write Speed/Power</td>
<td>~Flash → Higher</td>
<td>Fastest latency, high power</td>
<td>Fast – RAM like</td>
</tr>
<tr>
<td>Bit Alterable?</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Read Endurance</td>
<td>Unlimited</td>
<td>Unlimited</td>
<td>Limited</td>
</tr>
<tr>
<td>Write Endurance</td>
<td>High</td>
<td>Unlimited</td>
<td>Higher</td>
</tr>
<tr>
<td>Logic Integration</td>
<td>Easiest</td>
<td>Harder</td>
<td>Easier</td>
</tr>
<tr>
<td>Application Reach</td>
<td>Flash + Most RAM + Embedded Memory</td>
<td>Embedded/Cache Memory</td>
<td>Embedded Memory</td>
</tr>
</tbody>
</table>

Source: Intel
Overview of Emerging Memory Alternatives
- Near Term Candidates
- Longer Term, Litho Defined Candidates
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Future Research Trend: Extending in Multiple Layers

- Litho defined memories seeking to extend scaling in vertical dimension
  - Industry work on everything from NAND to polymer

- Ideal Effective Cell Area:
  \[ Z = \frac{4F^2}{y} \]
  Where \( y \) = # of layers

- Challenge is manufacturing cost of multiple layers

R&D Example (circa 2003):
Read/Write Eight Layer Memory using Ferroelectric Polymer

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# Other NVM Candidates in the Longer Term Research & Discovery Phase (Part 1 of 2)

<table>
<thead>
<tr>
<th>Material</th>
<th>Structure</th>
<th>Description</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>RRAM</td>
<td><img src="image" alt="RRAM Structure" /></td>
<td>Resistance change in CMO (usually crosspoint and multilayer)</td>
<td>Resistance change based on an applied field</td>
</tr>
<tr>
<td>Ferroelectric Polymer</td>
<td><img src="image" alt="Ferroelectric Polymer Structure" /></td>
<td>Cross-point, multi-layer capacitive storage in Polymer</td>
<td>Change in capacitance based on an applied field</td>
</tr>
<tr>
<td>Resistive Polymer</td>
<td><img src="image" alt="Resistive Polymer Structure" /></td>
<td>Cross-point, multi-layer resistive storage in Polymer</td>
<td>Change in resistance based on an applied field</td>
</tr>
</tbody>
</table>

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Source: Intel
### Other NVM Candidates in the Longer Term Research & Discovery Phase (Part 2 of 2)

<table>
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<tr>
<th>Material</th>
<th>Structure</th>
<th>Description</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmable Metallization</td>
<td><img src="Image" alt="Silver Dissolved in Chalcogenide" /></td>
<td>Silver Dissolved in Chalcogenide</td>
<td>Field Driven “Electroplating”</td>
</tr>
<tr>
<td>Carbon Nanotube</td>
<td><img src="Image" alt="Cross Point Array of Nanotubes Switches" /></td>
<td>Cross Point Array of Nanotubes Switches</td>
<td>Electrostatic Attraction + Van der Waals Adhesion</td>
</tr>
<tr>
<td>Molecular</td>
<td><img src="Image" alt="Molecules in CrossPoint Array" /></td>
<td>Molecules in CrossPoint Array</td>
<td>Voltage Driven Change in electronic states in Redox</td>
</tr>
</tbody>
</table>

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Seek & Scan Probe Storage

Seek & Scan Probe (SSP):
- MEMs device with nanopositioned probe tips
- Employs alternative storage media
- Molecular level storage is ultimate goal

Best achievable memory density projections over time:
A) IBM Millipede today
B) Improved storage media
C) Full molecular memory storage capability

Source: Intel

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Scaling: Not by Lithography

- Bit size: Determined by Media & Tip interactions
- Track Pitch/Position: Determined by Nano-positioning
  - Motor resolution < 1nm resolution reported
- Tip Scaling: Determined by tip field focusing
  - Tip shape & media fields & current distribution

~10 nm bit on PCM media via AFM

Source: Intel
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Conclusions
Key Findings

- Flash memory technology working to address scaling challenges
- New memory technology is rare
  - Last to break beyond a niche was flash ~20 years ago
- Phase Change Memory is the most promising of near-term candidates
- Multi-level, 3D and MEMS devices hold most promise for the future
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