Flash Memory Trends & Perspectives

Presented by:
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Semiconductor Insights
1. Introduction of Semiconductor Insights
2. NAND Technology
   • Technology Hurdles
   • NAND Device Trends (Die Size, Cell Size, Architecture)
   • MLC vs SLC
3. NOR Technology
   • NOR Device Trends (Die Size, Architecture)
   • High Level Device Analysis
4. Flash Processes
5. Trends & Perspectives
• World’s leading technical advisor to global microelectronics industry
• Support clients with in-depth technical investigation of IC’s and electronic systems to…
  – Assert their IP rights
  – Develop & commercialize new technologies and products
• Clients
  – Major electronics and semiconductor corporations in Japan, Korea, Taiwan, Europe, & North America and their representing law firms
TECHinsights helps technology companies…
   - Solve technical problems to:
     - Build competitive position
     - Assess new market entry
   - Memory is one of eight areas of expertise
   - Memory expertise includes
     - NAND Flash
     - NOR Flash
     - DRAM
     - eMemory
     - SRAM
     - New & Other Technology Related to Silicon Data Storage
NAND Technology Hurdles

• NAND competes on density and cost, reliability is not as good as NOR but use ECC.
  – Use advanced processes
  – Minimize Die Size
  – Use MLC technology

• MLC Technology
  – Difficult to sense voltage levels as technology scales
  – Reliability is not as good as SLC but good enough
NAND Die Size Trends – Small Die, Low Cost

Die Size

- Micron Competitive (90nm)
- Samsung 90nm MLC & 73nm SLC
- Hynix 73nm
- Toshiba 70nm
- Samsung 65nm
- Toshiba 70nm
- Optimized 2G Toshiba

Density

- Samsung 1
- Samsung 2
- Samsung 3
- Toshiba 1
- Toshiba 2
- Micron
- Hynix/ST

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NAND Flash Cell Sizes

Cell Size (um²) vs. Process Generation (nm)

4F2 Cell Size
0.012um² at 55nm
## Evaluated Leading-edge NAND Flash Devices

<table>
<thead>
<tr>
<th>Manuf.</th>
<th>Part Number</th>
<th>Technology</th>
<th>Die Capacity (Gbit)</th>
<th>Die Size (mm²)</th>
<th>Die Density (Mbit/ mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Samsung</td>
<td>K9F4G08U0A</td>
<td>65nm SBC</td>
<td>4</td>
<td>131</td>
<td>31.3</td>
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<tr>
<td>Samsung</td>
<td>K9G4G08U0M</td>
<td>90nm MLC</td>
<td>4</td>
<td>156</td>
<td>26.2</td>
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<tr>
<td>Samsung</td>
<td>K9F4G08U0M</td>
<td>73nm SBC</td>
<td>4</td>
<td>155</td>
<td>26.4</td>
</tr>
<tr>
<td>Toshiba</td>
<td>TH58NVG3D4BTGI0</td>
<td>90nm MLC</td>
<td>4</td>
<td>138</td>
<td>29.0</td>
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<tr>
<td>Hynix/ST</td>
<td>NAND04GW3B2BN6</td>
<td>73nm MLC</td>
<td>4</td>
<td>144</td>
<td>28.4</td>
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<tr>
<td>Toshiba</td>
<td>TC58NVG3D4CTG00</td>
<td>70nm MLC</td>
<td>8</td>
<td>145</td>
<td>56.5</td>
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</tbody>
</table>
NAND Flash Architecture Convergence

Common Architectural Layout

Samsung 2Gbit 90nm
Micron 2Gbit 90nm
Toshiba 4Gbit 90nm
Samsung 4Gbit 73nm
Toshiba 8Gbit 70nm
Hynix 4Gbit 73nm
Samsung 4Gbit 65nm

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SLC
- Simpler programming algorithm
- More reliable
- More expensive

MLC
- Complex programming algorithm
- Cost advantages
- Less reliable
Memory States Illustration

Two phase scheme to reduce programming time
NOR Technology Hurdles

• NOR used in wide variety of applications (Ease of use and increased reliability)
• Reliability is key for NOR
  – Technology scaling
  – MLC sensing in upcoming generations
• Density
NOR Flash Die Size/Density Trends

Die Size mm² vs. Density (Mb)

- Intel MLC
- Intel SLC
- Spansion
- Samsung
- ST Microelectronics

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Intel 64M SLC Die Sizes

Die Size (mm²) vs. Process Generation

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<table>
<thead>
<tr>
<th>Device</th>
<th>Part Number</th>
<th>Die Size (mm²)</th>
<th>Die Efficiency (Mb/mm²)</th>
<th>Process (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spansion 3.0 V 512 Mb (MBC) trapped charge</td>
<td>GL512N11FAE01</td>
<td>74.69</td>
<td>6.85</td>
<td>110</td>
</tr>
<tr>
<td>Spansion 1.8 V 256 Mb (MBC) trapped charge</td>
<td>WS256NOLBAW01</td>
<td>50.35</td>
<td>5.08</td>
<td>110</td>
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<tr>
<td>Intel 1.8 V 256 Mb (MLC) floating gate</td>
<td>28F256L18</td>
<td>47.85</td>
<td>5.35</td>
<td>130</td>
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<tr>
<td>Intel 1.8 V 512 Mb (MLC) floating gate</td>
<td>28F512EM</td>
<td>43.8</td>
<td>11.69</td>
<td>90</td>
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<tr>
<td>Intel 1.8 V 64 Mb floating gate</td>
<td>28F640EW</td>
<td>15.12</td>
<td>4.24</td>
<td>90</td>
</tr>
</tbody>
</table>
Intel Flash Products

Intel L18 (130nm) 47.9mm²

Intel M18 (90nm) 43.8mm²

Intel Wireless (90nm) 5.1mm²
Spansion Mirror Bit Devices

Spansion 3.0v
110nm 512Mb

Spansion 1.8v
110nm 256Mb

AMD 3.0v
230nm 64Mb
Scaling Challenges

- Alignment
- Coupling ratio
- Tunnel dielectric thickness
- Cross-talk
Flash Cell Types

SA-STI Cell
- Used by most manufacturers up to 90nm node and some beyond
- Misalignment Problems

Fully Aligned Cell
- Used by Toshiba at 90nm and Samsung at 73nm and 65nm
- No misalignment problems
Peripheral Gate Stack

No ONO

Contact Window

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Floating Gate (StrataFlash) vs NROM (Mirrorbit)

- **Floating Gate (StrataFlash)**
  - Store electrons in floating gate
  - Multi-Level Sensing

- **NROM**
  - Storage in Nitride layer
  - 2 bits per cell but two physical locations in cell
• NAND architecture converging although some variations in design

• 1st Generation NAND sizes between 135mm² & 160mm²

• MLC manufacturers increasing, cost savings but added complexity & less reliability

• Cell basic structure unchanged through several generations in NAND with SA-STI, manufacturers adopting completely self aligned cell others likely to follow

• Tunnel oxide and inter-poly dielectric almost unchanged up to 90nm generation
• We believe that the current floating gate planar cell structure can be scaled to the 45 nm node - More revolutionary technologies may be required to go beyond:
  – TODAY
    • Both MLC and NROM technologies are viable
    • FRAM gaining acceptance in niche markets
    • Matrix OTP memory – disposable digital film
  – TOMORROW
    • Will MLC or NROM technology scale better
    • PCRAM – Devices soon?
    • Non-planar cell structure (FinFET or recessed-channel)
    • Samsung recently announced 50nm 16G flash memory die using 3D-transistor architecture (which is probably Samsung’s proprietary recessed-channel technology)
    • Nanocrystal technology ~ Electrons trapped into silicon nanocrystals that act as nano-floating gates
Questions

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