Flash Standards for Embedded Systems

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Abstract

- OEMs are demanding that Flash-based interfaces migrate from a lawless "wild, wild West" frontier to one of defined standards to support interoperability among vendors and to simplify product design, test, and validation.

- Take a look at the standards behind controller-less NAND Flash interfaces like the traditional, asynchronous NAND interface and the high-speed, synchronous NAND interface, as well as the standards for controller-based interfaces like BA NAND, e-MMC™, and UFS.
Agenda

- No standards: the “wild, wild, West”
- Flash-based interface standards
- The interface “round-up”
No Standards: The “Wild, Wild West”

- Standards are needed for device interoperability
- No standards lead to incompatibilities—the “wild, wild West,” which was characterized by:
  - Gunfights and shootouts
  - Lawlessness
  - Robbers
A “Wild, Wild West” Example: NAND Flash

- The NAND Flash interface is a great example of how an interface with no standard became fragmented
  - Lack of consistent device and feature identification
  - Incompatible array architectures and addressing schemes
  - Different command sets
  - Inconsistent device behavior and status

- Result
  - Firmware bandages
  - Long product development/qual cycles
  - Lost revenue from longer time to market
  - The single source trap
Agenda

- No standards: the “wild, wild, West”
- Flash-based interface standards
- The interface “round-up”
## Flash-Based Embedded Interface Standards

<table>
<thead>
<tr>
<th>Standards Organization</th>
<th>Embedded Interface</th>
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</thead>
<tbody>
<tr>
<td>MMCA/JEDEC</td>
<td>e-MMC</td>
</tr>
<tr>
<td>JEDEC</td>
<td>UFS</td>
</tr>
<tr>
<td>ONFI</td>
<td>NAND</td>
</tr>
<tr>
<td></td>
<td>Source-synchronous NAND</td>
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<tr>
<td></td>
<td>BA NAND</td>
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<tr>
<td>SDA</td>
<td>eSD</td>
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</tbody>
</table>
Two Types of Interfaces

- **Raw**
  - The NAND memory is directly controlled by the host processor/controller
  - The host processor provides ECC, wear-leveling, and block management
  - The host processor deals with NAND architecture differences including page size, block size, # of planes, array performance
  - Lower cost per bit

- **Managed**
  - The NAND memory is buffered by an interface controller in the same package as the NAND
  - The interface controller provides ECC, wear-leveling, and block management
  - The interface controller hides the NAND architecture and provides fixed data sector sizes to the host
  - Lower up-front development cost
Raw vs. Managed Interface Examples

- Raw interface
- Managed interface
Standard Raw and Managed Interfaces

- **Raw**
  - Asynchronous NAND
  - Source-synchronous NAND

- **Managed**
  - BA NAND
  - e-MMC
  - eSD
  - UFS
Open NAND Flash Interface (ONFI)

- Asynchronous NAND Flash interface
  - First defined in ONFI 1.0
  - Up to 50 MB/s interface
  - The ONFI 2.0 standard is backward compatible to ONFI 1.0

- Source-synchronous NAND Flash interface
  - Defined in ONFI 2.0
  - Up to 133 MB/s interface
  - Even faster interface speeds coming in ONFI 2.1
The ONFI Round-Up

- NAND consistencies with ONFI
  - Device identification using the parameter page
  - Array architecture and addressing
  - Command set
  - Timing modes and parameters
  - ECC and endurance
  - Factory-marked bad blocks
  - Device behavior and status
  - Packaging
ONFI is a Standard, Not the Sheriff

- The ONFI specification does not mandate device architectures
  - Page size
  - Number of pages per block
  - Number of blocks
  - Number of planes
  - Amount of ECC required
  - Array performance

- They are discoverable by the host in the parameter page
ONFI Block Abstracted NAND

- BA NAND uses the same NAND interface (signals, electricals, packaging)
- Uses a different protocol
- Data is stored in sectors
e-MMC

- Interface and packaging standardized by MMCA and JEDEC
- MMC interface found already on many wireless controllers today
- e-MMC is supported by most NAND vendors
  - Hynix (e-NAND)
  - Micron (e-MMC™)
  - Samsung (moviNAND™)
  - Toshiba (eMMC NAND)
- Interface standardized by SDA; packaging compatible with JEDEC

- SD interface found already on many wireless controllers today

- Though a standard interface, it is not an open standard—not publicly published

- Not royalty-free
The interface “round-up”
## Raw Interface Comparison

<table>
<thead>
<tr>
<th></th>
<th>Async NAND</th>
<th>Source-Sync NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage</strong></td>
<td>3.3V/1.8V</td>
<td>3.3V/1.8V</td>
</tr>
<tr>
<td><strong>Data bus width</strong></td>
<td>X8, x16</td>
<td>x8</td>
</tr>
<tr>
<td><strong>Max clock</strong></td>
<td>50 MHz</td>
<td>66 MHz DDR</td>
</tr>
<tr>
<td><strong>Max transfer rate</strong></td>
<td>50 MB/s</td>
<td>133 MB/s</td>
</tr>
<tr>
<td><strong>Annual membership cost</strong></td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td><strong>Supplier support</strong></td>
<td>Hynix, Intel, Micron</td>
<td>Intel, Micron, more coming…</td>
</tr>
<tr>
<td><strong>Package standard</strong></td>
<td>JEDEC/ONFI</td>
<td>ONFI</td>
</tr>
</tbody>
</table>

*TSOP package references JEDEC mechanical drawings.*
## Managed Interface Comparison

<table>
<thead>
<tr>
<th></th>
<th>BA NAND</th>
<th>eSD</th>
<th>e-MMC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage</strong></td>
<td>3.3V/1.8V</td>
<td>3.3V/1.8V</td>
<td>3.3V/1.8V</td>
</tr>
<tr>
<td><strong>Data bus width</strong></td>
<td>x8</td>
<td>x1, x4</td>
<td>x1, x4, x8</td>
</tr>
<tr>
<td><strong>Max clock</strong></td>
<td>50 MHz</td>
<td>50 MHz</td>
<td>52MHz</td>
</tr>
<tr>
<td><strong>Max transfer rate</strong></td>
<td>50 MB/s</td>
<td>25 MB/s</td>
<td>52 MB/s</td>
</tr>
<tr>
<td><strong>Annual membership cost</strong></td>
<td>None</td>
<td>Yes</td>
<td>None</td>
</tr>
<tr>
<td><strong>Supplier support</strong></td>
<td>Coming</td>
<td>Toshiba (eSD)</td>
<td>Micron (e-MMC™)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sandisk (iNAND)</td>
<td>Samsung (mobiNAND™)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Toshiba (eMMC)</td>
</tr>
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<td></td>
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<td>JEDEC</td>
<td>JEDEC</td>
</tr>
</tbody>
</table>

*Follows JEDEC JC64.1 NAND card/module package format.*
Upcoming Managed Interfaces

- **UFS (JEDEC)**
  - Uses ring topology for data transmission
  - Low voltage, high performance
  - One-to-many differential pairs for scalable throughput
  - Protocol optimized for storage interfaces

- **USB 3.0 (USB-IF)**
  - USB 3.0 controller may become embedded with NAND memory in the same package
  - Low voltage, high performance
  - One differential pair
  - Protocol optimized for many interfaces
Embedded Flash-Based Interface Standards Organizations

- MultiMediaCard Association (MMCA)

- JEDEC

- Open NAND Flash Interface (ONFI) Workgroup

- SD Card Association (SDA)

- USB Implementers Forum
About Michael Abraham

- Manager of Micron’s NAND Flash Applications Engineering group
- B.S. in Computer Engineering from Brigham Young University
- Micron’s technical representative in ONFI and JEDEC for NAND Flash
- Key role in defining and standardizing the new high-speed NAND interface within Micron and at ONFI